MIPS CPU INSTRUCTIONS *for COSC2021*

Arithmetic Family (14)		**TYPE 0x**	**ORDER**
add(u)	reg0, reg1, reg2	R 20 (21)	1,2,0
addi(u)	reg0, reg1, imm	I 08 (09)	1,0
sub(u)	reg0, reg1, reg2	R 22 (23)	1,2,0
mult(u)	reg1, reg2	R 18 (19)	1,2
div(u)	reg1, reg2	R 1A (1B)	1,2
slt(u)	reg0, reg1, reg2	R 2A (2B)	1,2,0
slti(u)	reg0, reg1, imm	I 0A (0B)	1,0
Logical Family (13)			
and	reg0, reg1, reg2	R 24	1,2,0
andi	reg0, reg1, imm	I 0C	1,0
or	reg0, reg1, reg2	R 25	1,2,0
ori	reg0, reg1, imm	I 0D	1,0
xor	reg0, reg1, reg2	R 26	1,2,0
xori	reg0, reg1, Imm	I 0E	1,0
nor	reg0, reg1, reg2	R 27	1,2,0
sllv	reg0, reg1, reg2	R 04	2,1,0
sll	reg0, reg1, imm	R 00	zero,1,0
srlv	reg0, reg1, reg2	R 06	2,1,0
srl	reg0, reg1, imm	R 02	zero,1,0
srav	reg0, reg1, reg2	R 07	2,1,0
sra	reg0, reg1, imm	R 03	zero,1,0
Jump Family (3)			
j	imm	J 02	
jr	reg	R 08	reg,0…
jal	imm	J 03	
Branch Family (6)			
bgtz	reg, imm	I 07	reg,zero
bgez	reg, imm	I 01	reg,one
bltz	reg, imm	I 01	reg,zero
blez	reg, imm	I 06	reg,zero
beq	reg1, reg2, imm	I 04	1,2
bne	reg1, reg2, imm	I 05	1,2
Load / Store Family (8)			
lw	reg0, imm (reg1)	I 23	1,0
lh(u)	reg0, imm (reg1)	I 21 (25)	1,0
lb(u)	reg0, imm (reg1)	I 20 (24)	1,0
sw	reg0, imm (reg1)	I 2B	1,0
sh	reg0, imm (reg1)	I 29	1,0
sb	reg0, imm (reg1)	I 28	1,0
"Other" Family (6)			
lui	reg, imm	I 0F	zero,reg
syscall		R 0C	
mflo	reg	R 12	0,0,reg
mtlo	reg	R 13	reg,0,0
mfhi	reg	R 10	0,0,reg
mthi	reg	R11	reg,0,0

REGISTERS

0	**0**
1	**at**
2	**v0**
3	**v1**
4	**a0**
5	**a1**
6	**a2**
7	**a3**
8	**t0**
9	**t1**
10	**t2**
11	**t3**
12	**t4**
13	**t5**
14	**t6**
15	**t7**
16	**s0**
17	**s1**
18	**s2**
19	**s3**
20	**s4**
21	**s5**
22	**s6**
23	**s7**
24	**t8**
25	**t9**
26	**k0**
27	**k1**
28	**gp**
29	**sp**
30	**fp**
31	**ra**

SYSCALL

Service	**v0**	**Send**	**Return**
Print int	1	a0	
Print float	2	f12	
Print double	3	f12	
Print string	4	a0	
Read int	5		v0
Read float	6		f0
Read double	7		f0
Read string	8	a0/1	
Allocate	9	a0	v0
Print char	11	a0	

ASCII CODE

```
0-9 start at 48 or 0x30
A-Z start at 65 or 0x41
a-z start at 97 or 0x61
' ' space at 32 or 0x20
```