CSE3215 Embedded Systems Laboratory

Lab5 – Reaction Timer VLSI Implementation

Objective

Initial marketing analysis of the MCU based reaction timer you designed in Lab3 showed promise and is worth bringing to market. The final production version however is to be a total VLSI implementation. The objective of this lab is to prototype this VLSI design using the Cyclone II FPGA on the Altera DE2.

Design Specifications

As in Lab3 the reaction timer measures and displays the reaction time of a subject's response to a visual stimulus. This lab involves an Altera DE2 board implementation with design specifications as follows:

Functional Specifications

- The reaction timer must measure reaction times up to 9999ms.
- Measurements are displayed on the 7-segment display present on the DE2, with leading zeros blanked i.e. display " 67" not "0067".
- The system starts up in an idle state with the power up message "P000" displayed on the 7-segment display while waiting for the first reaction time measurement to be initiated.
- Pushbutton KEY2 is used to start a new reaction time measurement. Actuating KEY2 blanks the 7-segment display; the measurement itself does not start until the release of KEY2. Upon the release of KEY2 a random onset delay (500ms to 3sec) is started. After the stimulus onset delay is complete the stimulus led - "LED1" is pulsed for 100ms. Following the press of the response button (KEY0), the measured reaction time is displayed on the 7-segment display. If a valid response is not received within 9999ms after the stimulus led is first illuminated then the measurement is discarded and the value "E001" is displayed indicating an error condition. The system then waits for a reaction time measurement request.
- The reaction time is defined as the time interval between the initial display of the stimulus LED to the actuation of the response switch.

Design Constraints

The following is a list of constraints placed on the overall design of your reaction timer.

- All timers, display drivers, etc. must be implemented in Verilog and of your own design.

- The pushbutton switches *(KEY0...KEY3*) on the DE2 are already debounced using a Schmitt Trigger circuit. You do not need to design a "DEBOUNCE" module before using these switches in your design.

- The DE2 has two internal oscillators that produce 27MHz and 50MHz clock signals. Use any one of them in your design.

- The DE2 board has eight 7-segment displays. Refer to the DE2 Manual for a schematic diagram of the displays. Use the displays arranged in a group of four - *[HEX0..HEX3]* for this lab.

Reference Material

DE2 User Manual

Pre Lab

1. Design a Finite State Machine to describe your reaction timer. Implement your design in Verilog. Determine the *Inputs* and *Outputs* to your **fsm** module.

2. Draw a block diagram of your reaction timer.

Procedure

1. Ensure that you have set the DE2 to set all unused pins as "tri-state inputs" prior to burning your Verilog code onto the Altera. This prevents accidental burnouts as a result of an unused pin driving a "1" or "0" as output. If you are unsure how to do this ask the TA for assistance.

2. Program and debug your design using the oscilloscope and/or logic analyzer to verify your measurements. You can use the expansion headers JP1 and JP2 on the Altera to debug your individual modules.

Evaluation

1. Prelab (including preliminary code) 20%
2. Lab demonstration, in-lab explanations and answers, debug and test approach 60%
3. Program/design documentation (code should be well documented but no report is required – submit electronically within 24 hours on Prism) 20%

Demonstrate your program to the T.A showing that it conforms to the design specifications. Part of this demonstration **must** be a measurement of the reaction time using the oscilloscope or logic analyzer.

BONUS

To make your reaction timer more challenging for the subject, include another led (*LED6*) and switch (*KEY3*) in your design. As in Lab 3 only one of the leds is lit to provide the reaction stimulus, and the appropriate button (*KEY0* for *LED1* and *KEY3* for *LED6*) must then be depressed to measure the response of the subject. The LED must be chosen randomly.