Name: _____
CSE ID: _____ Student Number: _____ **ID: A**

Midterm Test - CSE 2021 - Fall 2011

Instructions

- This is a closed book, 80 minutes test.
- The MIPS reference sheet may be used as an aid for this test.
- An 8.5" x 11" "Cheat Sheet" may also be used as an aid for this test. MUST be original handwriting.
- This is a question/answer booklet: Write your answers in the space provided and as indicated in each question. Use the backside for scratch work. *Do not* hand in anything other than this booklet.
- Fill in your personal data in the box below *before the start of the test*. *Do not* turn this page over until the instructor has announced that you may do so.
- Keep your York photo ID (or any other acceptable photo ID) on the desk in front of you so that the instructor may inspect it without disturbing you.
- You may use ONLY those instructions that appear in the MIPS sheet. Whenever needed, assume that **the machine is little endian.**
- No questions during the exam. Write your final answer with a pen.

LAST NAME: _____

FIRST NAME: _____

STUDENT NUMBER: _____

PRISM LOGIN: _____

Question	Points	Mark
1	6	
2	4	
3	6	
4	14	
5	10	
TOTAL	**40**	

Name: _____ **ID: A**

1.
```
start:    addi $a0, $0, 15
          addi $t0, $0, 0
          addi $t1, $0, 3
again:    slt  $t2, $a0, $t1
          bne  $t2, $0, end
          add  $t0, $t0, $t1
          addi $t1, $t1, 3
          j    again
end:      add  $v0, $t0, $0
```

$t1 (in hex) =

$v0 (in decimal) =

2. Translate the number below into a radix of 16. Also assuming IEEE 754 format, what decimal number is represented by:

   1 01111101 00100000000000000000000

Number (in hex) =

Number (in decimal) =

Name: _____ **ID: A**

Problem

3. The figure below shows the schematic diagram of a NAND gate

Fig.1: Schematic diagram of the NAND gate

which has the following truth table

a	*b*	*c* = *a* NAND *b*
0	0	1
0	1	1
1	0	1
1	1	0

A NAND gate is a universal gate because any digital component can be implemented using NAND gates only. Implement (a) a NOT gate, (b) an AND gate, and (c) an OR gate using only NAND gates. You may use more than one NAND gate but no other type of gate may be used.

4. A binary-to-seven segment decoder is a logic circuit that converts a number expressed in binary to an appropriate code for the selection of segments in a display indicator illustrated in fig. 1.

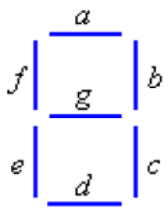

Fig. 1: Segment designation in a seven segment decoder

The binary-to-seven segment decoder has three input bits, say *x*, *y*, and *z* that hold the 3-bit binary representation of the number to be displayed. The seven outputs of the decoder (*a*, *b*, *c*, *d*, *e*, f, and *g*) select the corresponding segments in the display are shown in fig. 2 to highlight the numeric digits being displayed.

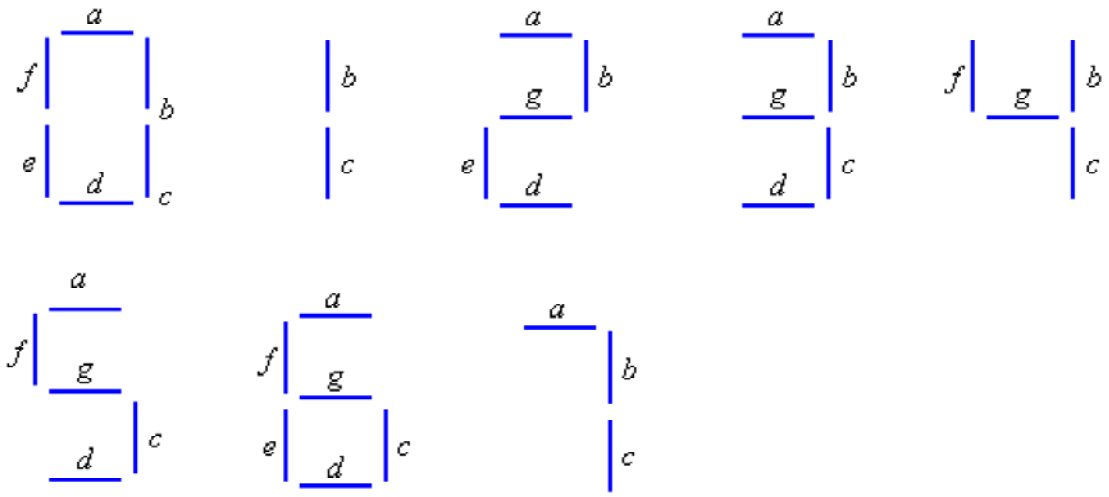

Fig. 2: Numerical designation for display of a number (from 0 to 7)

As an example, if binary number 001 is to be displayed, the binary inputs to the decoder are $x = y = 0$ and $z = 1$ with the outputs $b = c = 1$. The remaining five outputs *a*, *d*, *e*, *f*, and *g* are all 0. Answer the following questions the binary-to-seven segment decoder, shown in figs. 1 and 2.

a) [4 points] Fill in the truth table with three inputs (*x*, *y*, and *z*) and ONLY the first three outputs (*a, b, c*).

Inputs			*Outputs*		
x	*y*	*z*	*a*	*b*	*c*
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

b) [3 points] Based on the truth table drawn in a), derive a Boolean expressions for each of the first three outputs (*a, b, c*).

c) [3 points] Provide simplified Boolean expressions for each of the outputs in part (b).

c) [4 points] Using AND, OR, and NOT gates, draw digital circuits that implement the first 3 outputs (*a*, *b*, *c*) from the inputs (*x*, *y*, and *z*).

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5. Consider two different implementations, M1 and M2, of the same instruction set. There
are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and
M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their
frequencies (for a typical program) are as follows:

Instruction Class	M1 - Cycles/Instruction	M2 - Cycles/Instruction	Instruction Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

(a) [4 points] Calculate the average CPI for each machine, M1, and M2.

(b) [4 points] Calculate the average MIPS ratings for each machine, M1 and M2.

(c) [2 points] Which machine has a smaller MIPS rating ? Which individual instruction class CPI do you need to
change, and by how much, to have this machine have the same or better performance as the machine
with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the
slower machine)?

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Midterm Test - CSE 2021 - Fall 2011
Answer Section

SHORT ANSWER

1. ANS:

```
$t1 = 0x13

$v0 (in decimal) = 45
```

PTS: 1 OBJ: Section A

2. ANS:
1011 1110 1001 0000 0000 0000 0000 0000

B E 9 0 0 0 0 0

The decimal number

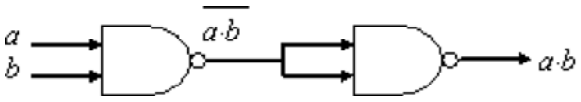
$= (-1)^1 * (1.001)_2 * (2^{(125-127)})$
$= (-1) * (1.125) * (0.25)$
$= -0.28125$

PTS: 1

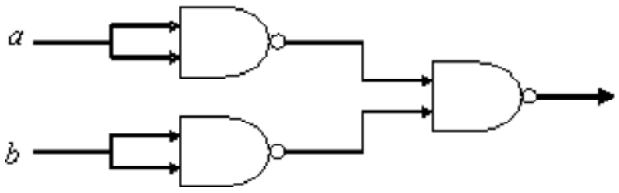
PROBLEM

3. ANS:
(a) NOT

(b) AND



(c) OR



PTS: 1 OBJ: Section B.1

4. ANS:

(a) The truth table for the binary-to-seven segment decoder is shown below (all 7 outputs are shown only a, b, c required for this question):

Inputs			Outputs						
x	*y*	*z*	*a*	*b*	*c*	*d*	*e*	*f*	*g*
0	0	0	1	1	1	1	1	1	0
0	0	1	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	1
0	1	1	1	1	1	1	0	0	1
1	0	0	0	1	1	0	0	1	1
1	0	1	1	0	1	1	0	1	1
1	1	0	1	0	1	1	1	1	1
1	1	1	1	1	1	0	0	0	0

(b) The Boolean expressions (for all 7, only a, b, c required) are given below

$$a = x'y'z' + x'yz' + x'yz + xy'z + xyz' + xyz,$$

$$b = x'y'z' + x'y'z + x'yz' + x'yz + xy'z' + xyz,$$

$$c = x'y'z' + x'y'z + x'yz + xy'z' + xy'z + xyz' + xyz,$$

$$d = x'y'z' + x'yz' + x'yz + xy'z + xyz',$$

$$e = x'y'z' + x'yz' + xyz',$$

$$f = x'y'z' + xy'z' + xy'z + xyz',$$

and $$g = x'yz' + x'yz + xy'z' + xy'z + xyz'.$$

(c) The expressions for *a*, *b*, *c* can be simplified fairly considerably:

$$a = x'z' + (x'y + xy')z + xy = x'z' + (x + y)(xy)'z + xy = x'z' + xz + yz + xy$$

$$a = y + x'z' + xz$$

$$b = x'z' + yz + (x'z + xz')y' = x'z' + yz + (x + z)(xz)'y' = (x + z)' + yz + (x + z)(xz)'y' = x'z' + yz + x'y' + z'y'$$

$$b = x' + y'z' + yz$$

$$c = x'y' + yz + xy' + xyz' = y' + y(z + xz') = y' + y(z + x) = x + y' + z$$

(d)The digital circuits can be drawn from the above Boolean expressions.

PTS: 1 OBJ: Section B.2

5. ANS:

(a) Calculate the average CPI for each machine, M1, and M2.

For Machine M1:

Clocks per Instruction = (60/100)* 1 + (30/100)*2 + (10/100)*4 = 1.6

For Machine M2:

Clocks per Instruction = (60/100)*2 + (30/100)*3 + (10/100)*4 = 2.5

(b) Calculate the average MIPS ratings for each machine, M1 and M2.

For Machine M1:

Average MIPS rating = Clock Rate/(CPI * 10^6) = (80 * 10^6) / (1.6*10^6) = 50.0

For Machine M2:

Average MIPS rating = Clock Rate/(CPI * 10^6) = (100 * 10^6) / (2.5*10^6) = 40.0

(c) Which machine has a smaller MIPS rating ? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Machine M2 has a smaller MIPS rating.

If we change the CPI of instruction class A for Machine M2 to 1, we can have a better MIPS rating than M1 as follows:

Clocks per Instruction = (60/100)*1 + (30/100)*3 + (10/100)*4 = 1.9

Average MIPS rating = Clock Rate/(CPI * 10^6) = (100 * 10^6) / (1.9*10^6) = 52.6

PTS: 1