CSE 3201 Digital Logic Laboratory

Lab 2: Boolean Logic and Digital Circuits

Objective

The objective of this lab is to gain experience implementing combinational circuits based on Boolean algebra.

Reference Material

Altera DE2 manual and tutorial, available from the course web site.

Pre-Lab

Background: In communications systems, a simple error detection scheme is the parity check. In parity generation, a bit is added to a sequence of transmitted bits in order to make the total number of bits even (even parity) or odd (odd parity). Parity generator and checkers enable this process.

Consider a circuit that produces a 1 if a bit pattern contains an odd number of 1's, otherwise it produces a 0. Such a function is called an odd function.

1. Develop the truth table and Boolean expression for a three-bit odd function. That is, 3 input bits to which a 4^{th} parity bit is appended.
2. What type of input gate does this function resemble?
3. Develop four Verilog implementations of this circuit based on:
    - Truth table realization (you may want to use an `always` block for this)
    - Product of maxterms structural implementation with AND and OR gates (canonical form)
    - The simplest structural implementation based on standard gates (AND, OR, XOR, NOR, NAND, XNOR, NOT)
    - Boolean functions and behavioural Verilog modelling.
4. Write a ***parity checker***. That is, develop Verilog code to check the parity of a sequence of four bits (i.e. three bits of data plus a parity bit $B_0B_1B_2B_3$). B_3 should be set (1) if the there is an **odd** number of 1's in the sequence (which **does not** include B_3), otherwise it should be 0.
5. Simulate your designs!

Before entering the lab ensure that for each design you have at a minimum:

- Truth tables, Boolean expressions and other design aids.
- Fully documented Verilog source
- Test patterns and/or a testing strategy

If you are not prepared for the lab you will not be allowed to start. The two-hour lab time slots are strictly enforced and you must be prepared in order to complete the lab in the allotted time.

In Lab Procedure

1. The DE2 board contains toggle switches and LEDs among the collection of external circuitry. These are useful for stimulating the inputs and displaying the outputs of circuits we design. Create a small Verilog based circuit that maps SW0 through SW4 to the correspondingly numbered red LEDs. Remember to assign the pins appropriately. Program the chip and verify that your circuit works.

2. For each of your odd-function designs, download and verify your circuits. All the circuits can be implemented at once – use SW0-2 for the truth table, SW4-6 for the canonical form, SW8-10 for the gate version and SW12-14 for Boolean function. Use LEDR0, 4, 8, and 12 for the respective outputs. Try all valuations of the inputs. When you are satisfied that all your designs work demonstrate them to your TA.

3. Program the chip with your **parity checker** design. Verify that the circuit works correctly. Demonstrate your design to the TA when you are satisfied it is correctly working.

The implemented circuits must be demonstrated to the TA who will note a completed lab and ask questions about your design. **When implementing the circuit be sure to use the switches and lights to make it easy to demonstrate your circuits.**

Evaluation

Lab demonstration, in-lab explanations and answers, debug and test approach.