# Dept. of and Electrical Engineering & Computer Science
# CSE4201 – Computer Architecture
# HW 1
# Due Oct. 1, 2013

1. 1.11 From the textbook
2. 1.15 From the textbook
3. 1.16 From the textbook

4. A MIPS like pipeline has the following stages

IF ID EX1 EX2 MEM1 MEM2 WB

The data is available from the ALU and memory after the second stage
We can read and write a register in the same cycle (writing in the first half, and reading in the second half)
There is forwarding from the output of the second memory stage to the input of the first EX stage only. No other forwarding is allowed.
How many cycles to execute (completely) the following code

```
LD      R1, 24(R2)
LD      R4, 36(R6)
ADD     R8, R4, R1
XOR     R10,R4,R7
SD      24(R2), R10
```