ENG2210
Electronic Circuits
Chapter 4 MOSFET

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Disclaimer: Most of the slides are skeletons that will be filled/modified in the lecture. Please do not assume that you can know the material just by reading the slides.

Chapter Objectives

- Learn the physical structure of the MOSFET and how it works.
- How to analyze circuits that contains MOSFET.
- How to obtain linear amplification from a nonlinear MOSFET.
- The three basic ways for connecting a MOSFET to construct amplifiers.
- Practical circuits for MOSFET.

MOSFET– Metal Oxide Semiconductor Field Effect Transistor

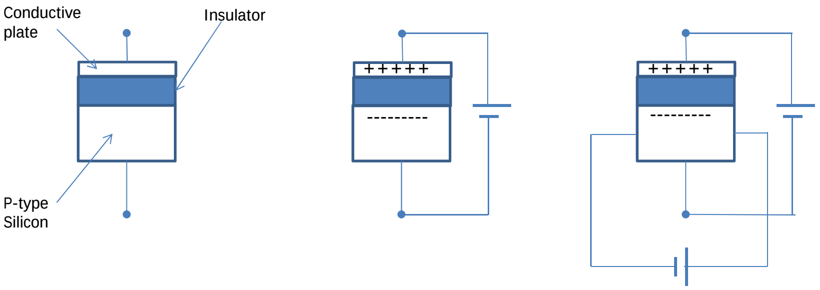
- Transistors (3 terminal devices) diodes are 2 terminal devices – more complicated.
- One terminal usually control the current between the other two terminals.
- Used in digital and analog circuits
- Mainly MOSFET and BJT (vast majority of IC's are MOSFET)
  - Smaller
  - Loss power than BJT – very important –

MOSFET

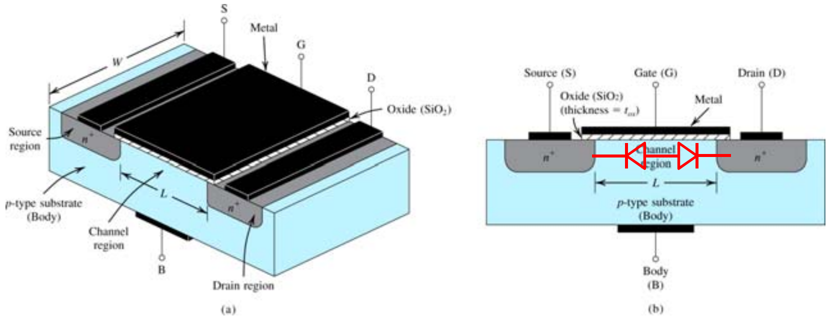
- This is not a course on semiconductor (nor this is a physics course). However, understanding how the device work is very important.

MOSFET

Not a real device, just to explain the idea



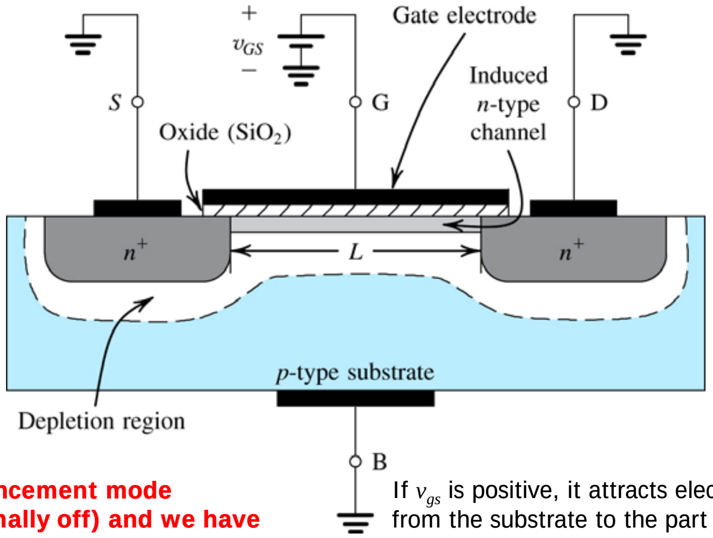
Gate is isolated (SiO2) no current from gate



(a) (b)

No current can flow between source and drain

Usually body contact is connected to the source

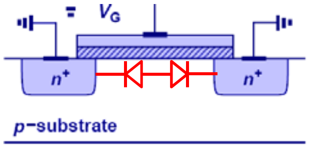


Enhancement mode (normally off) and we have to enhance it to be ON

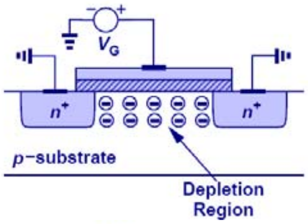
If v_{gs} is positive, it attracts electrons from the substrate to the part of the substrate next to the SiO2 creating a channel

MOSFET Operation

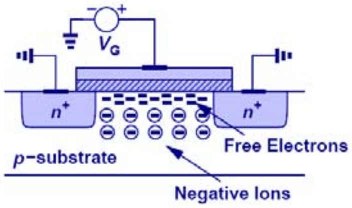
- We start by explaining how things work, then we use mathematics to derive equations.
- Start with n-MOS



V_G=0, because of the back-to-back diodes, no current flows from source to destination



V_G>0, Holes are repelled by the positive gate voltage and leaving behind negative ions forming a depletion region



As V_G increases (Threshold voltage), Electrons are attracted to the surface forming a channel where current **might** flow

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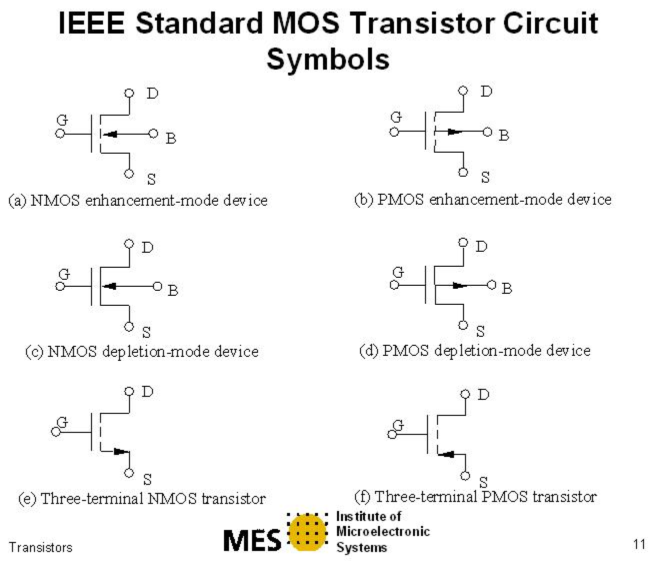

IEEE Standard MOS Transistor Circuit Symbols

(a) NMOS enhancement-mode device

(b) PMOS enhancement-mode device

(c) NMOS depletion-mode device

(d) PMOS depletion-mode device

(e) Three-terminal NMOS transistor

(f) Three-terminal PMOS transistor

Transistors

MES Institute of Microelectronic Systems

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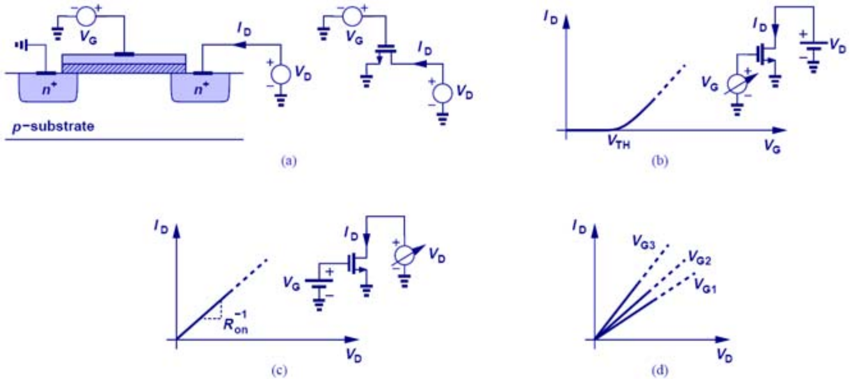
Source: http://people.seas.harvard.edu/~jones/es154/

NMOS Characteristics



- We can vary V_G and keeping V_D constant
- Or vary V_D and keeping V_G constant

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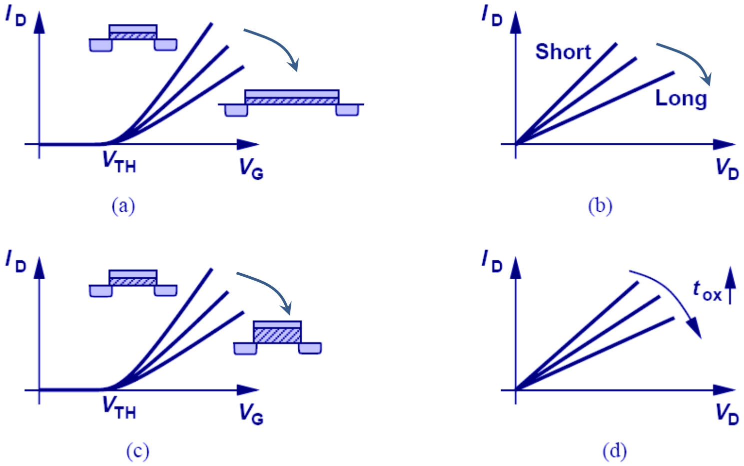
Effect of *L* and t_{ox}



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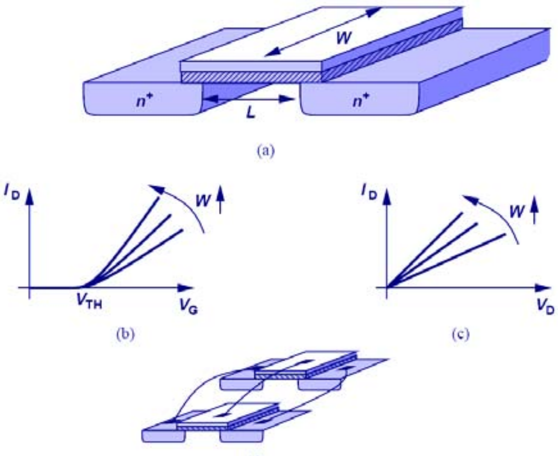
Effect of *W*



(a)

(b)

(c)

(d)

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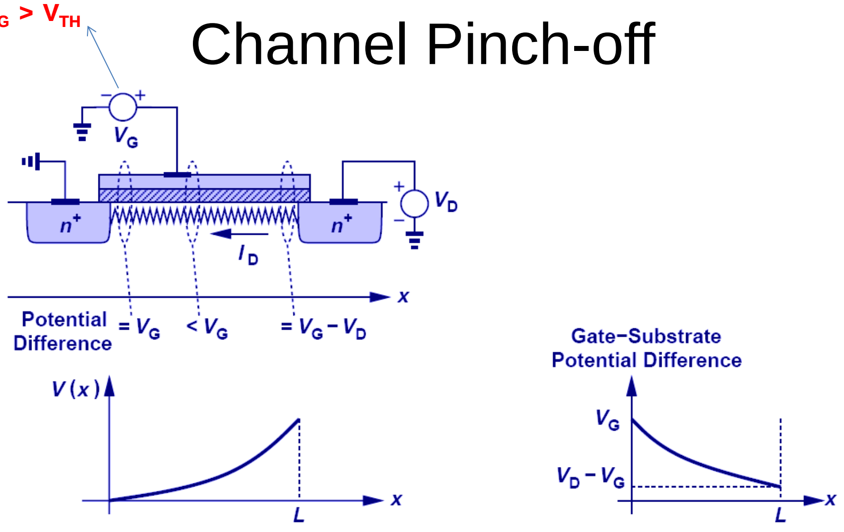
$V_G > V_{TH}$

Channel Pinch-off



(a)

(b)

The channel acts as a resistance, voltage increases from S ($V=0$) to D ($V=V_D$)

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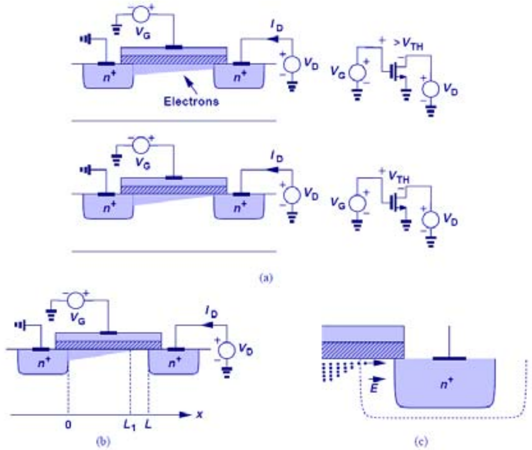
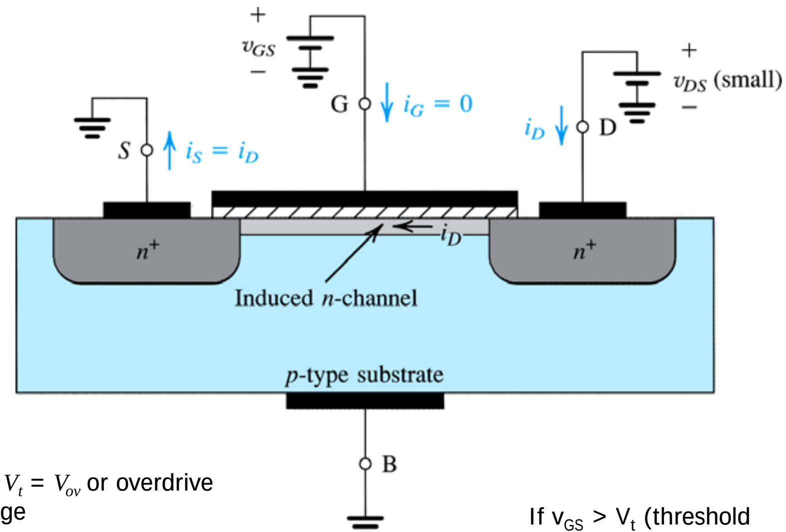
Channel Pinch-Off



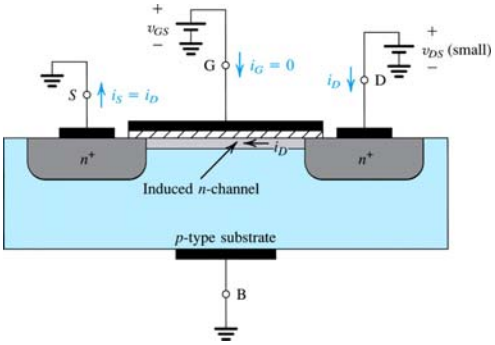
- As V_D increases, at some distance x, $V_G - V_D < V_{TH}$ and the channel does not exist anymore.
- Does that mean No current? No, The high electric field in the depletion region carry them through, but V_D does not control the current anymore (constant current source)



$v_{GS} - V_t = V_{ov}$ or overdrive voltage

If $v_{GS} > V_t$ (threshold voltage) and drain is positive, then current i_D can flow

Small v_{DS}



$$\frac{Q}{\text{Unit length}} = \frac{CV}{L} = \frac{(\varepsilon_{ox} A / t_{ox})V}{L}$$

$$\frac{Q}{\text{Unit length}} = C_{ox} W v_{ov}\ , \quad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$|E| = \frac{v_{DS}}{L}$$

$$\text{Electron drift velocity} = \mu_n |E| = \mu_n \frac{v_{DS}}{L}$$

$$i_D = \frac{Q}{\text{Unit length}} \times speed$$

$$i_D = C_{ox}\ W\ V_{ov} \times \mu_n \frac{v_{DS}}{L}$$

$$i_D = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov} \right] v_{DS}$$

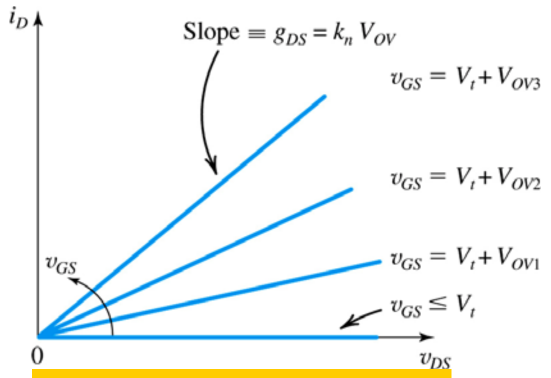
Small v_{DS}

$$i_D = \underbrace{\left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov} \right]}_{\text{Conductance}} v_{DS}$$

$$g_{DS} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov}}$$

Linear resistance



$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)V_{ov}\right]V_{DS}$$

Determined by the process technology=**K_n'**

Transistor Aspect Ratio

Overdrive voltage

K_n

Not Small v_{DS}

- As v_{DS} increases we can not assume a constant voltage between the gate and any point along the channel.
- The voltage at one end of the channel is 0, while at the other end is v_{DS}

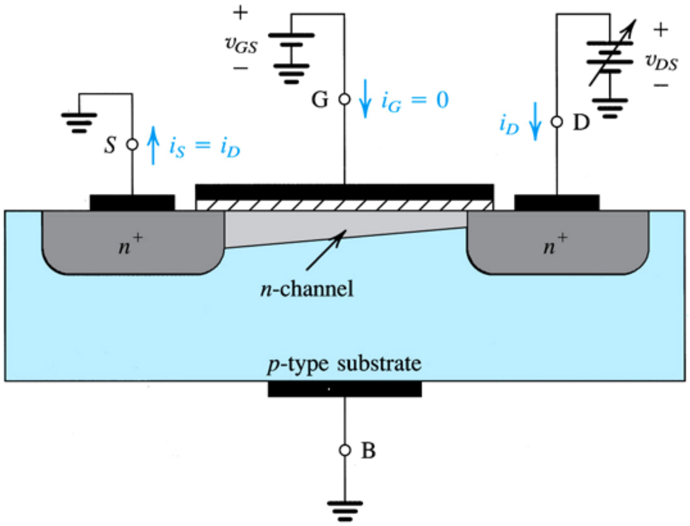


Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t; $v_{GS} = V_t + V_{OV}$.

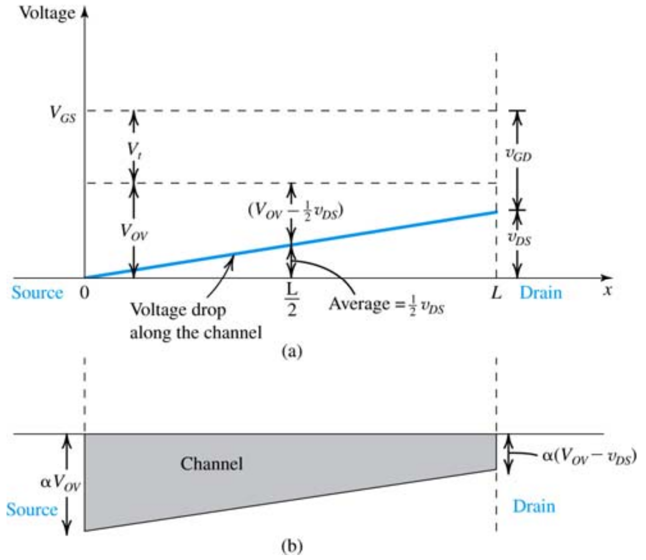


Figure 5.6(a) For a MOSFET with $v_{GS} = V_t + V_{OV}$, application of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2}v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. **(b)** The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to V_{OV}, that at the drain end is proporational to $(V_{OV} - v_{DS})$.

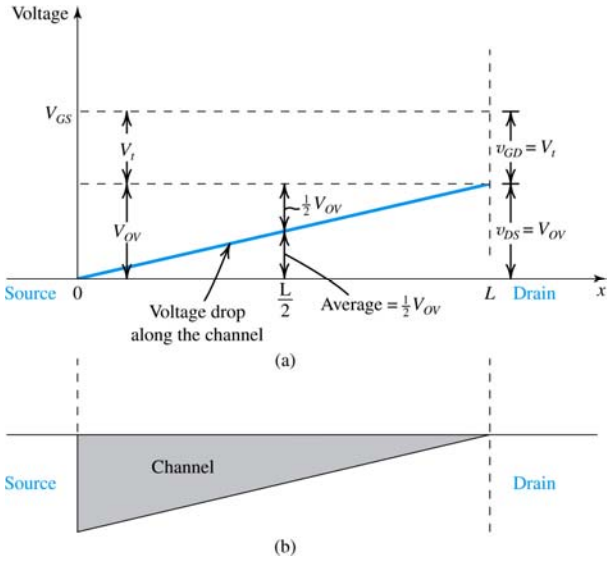
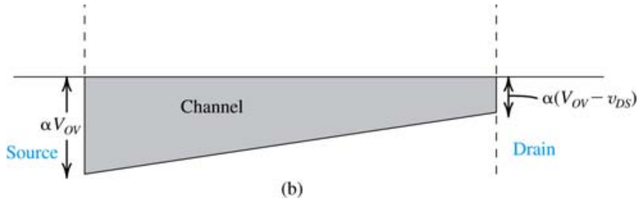


Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, as v_{DS} is increased to V_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{DSat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.



$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)V_{ov}\right]v_{DS}$$

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)\left(V_{ov} - \frac{1}{2}v_{DS}\right)\right]v_{DS}$$

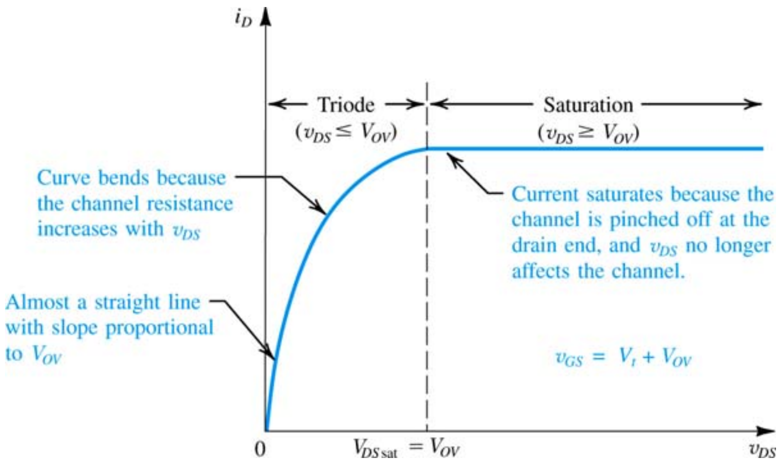
$$i_D = \left[k_n'\left(\frac{W}{L}\right)\left(V_{ov} - \frac{1}{2}v_{DS}\right)\right]v_{DS}$$

As v_{DS} increases the resistance increases and the current does not continue to grow with the same rate

$v_{DS} >= V_{ov}$

- As V_{DS} grows, the channel pinches off.
- When $v_{DS} = V_{ov}$ the channel depth is zero
- Increasing v_{DS} beyond that has no effect.
- The drain current saturates (saturation region)
- Electrons can still go through the depletion region

$$i_D = \frac{1}{2} k_n^{'} \left(\frac{W}{L} \right) V_{ov}^2$$



Curve bends because the channel resistance increases with v_{DS}

Almost a straight line with slope proportional to V_{OV}

Current saturates because the channel is pinched off at the drain end, and v_{DS} no longer affects the channel.

Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.

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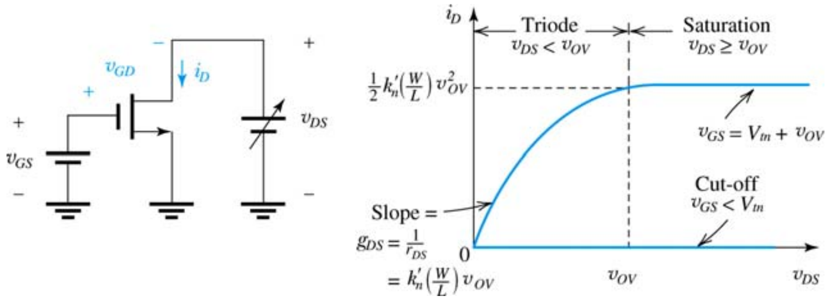


Table 5.1 Regions of Operation of the Enhancement NMOS Transistor

NMOS

Cut-off

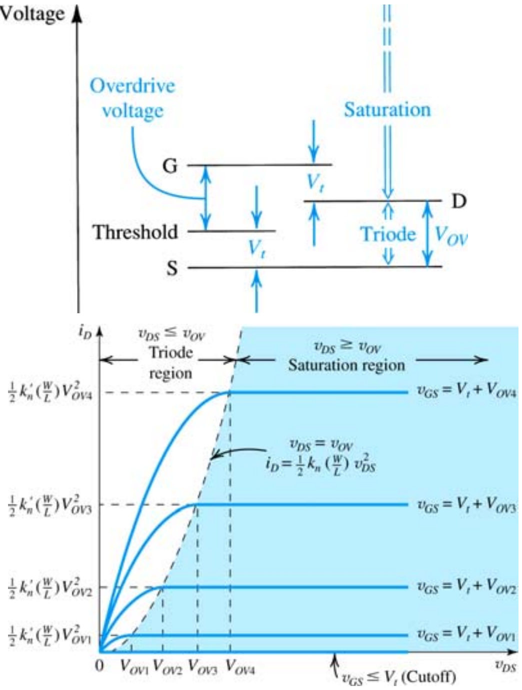
$$v_{GS} < V_{tn}$$

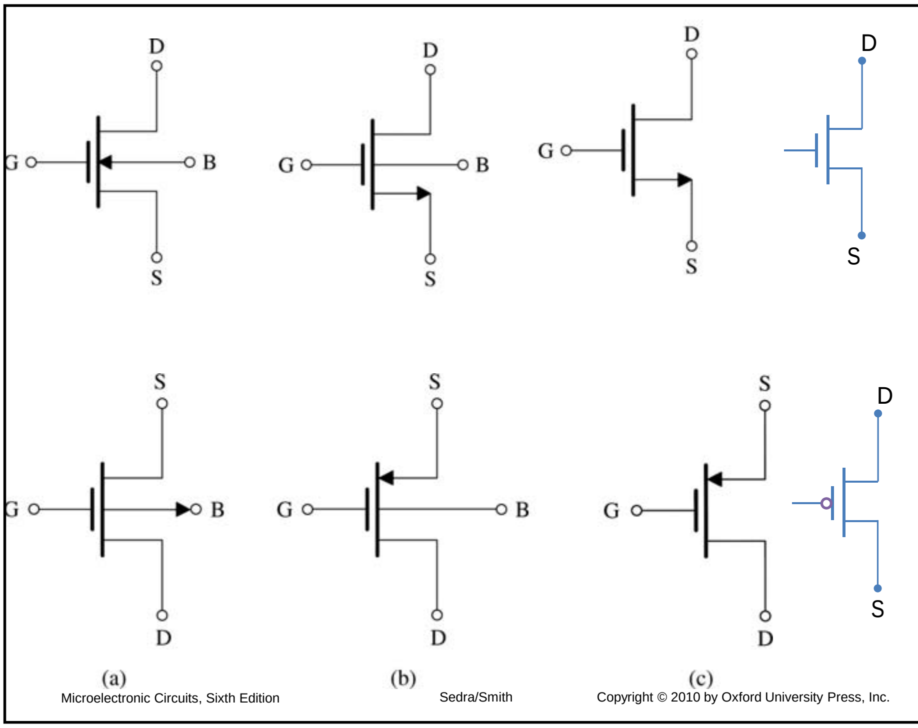
Saturation

$$v_{GS} > V_t$$
$$v_{DS} > v_{GS} - V_t$$
$$v_D - v_s > v_G - v_s - V_t$$
$$v_{GD} < V_t$$

Triode

$$v_{DS} < v_{OV}$$
$$v_{GD} > V_t$$





(a) (b) (c)

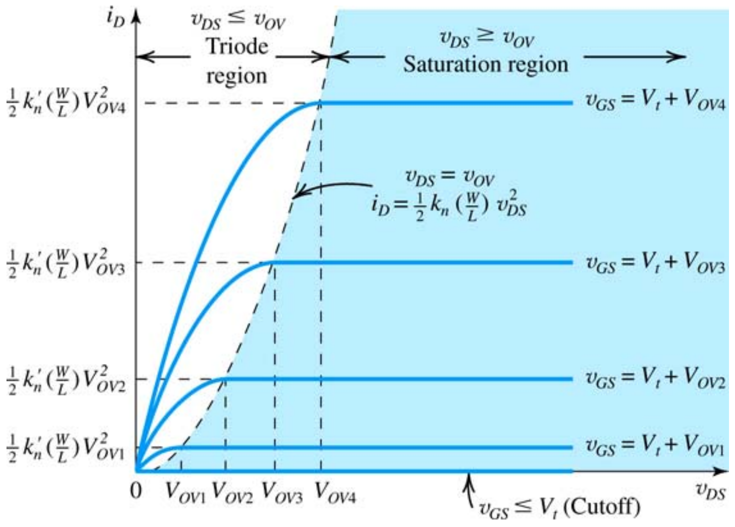


Figure 5.13 The i_D–v_{DS} characteristics for an enhancement-type NMOS transistor.

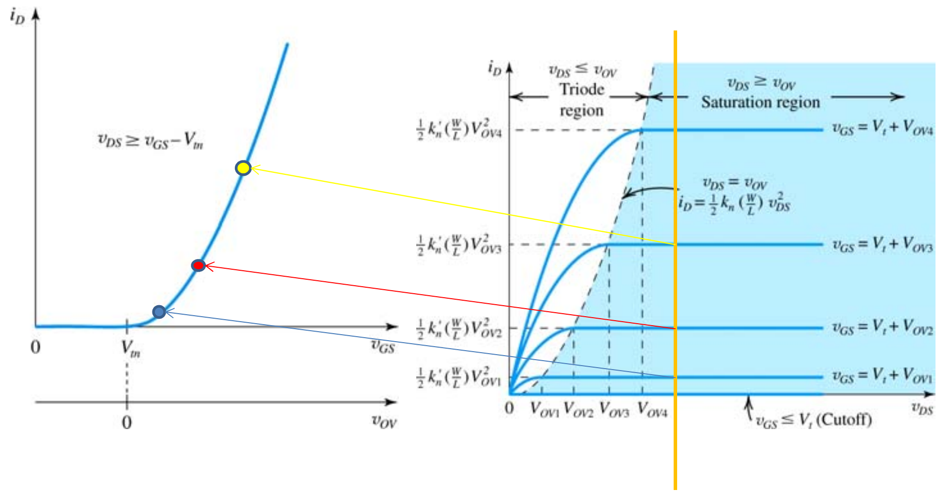


Figure 5.14 The i_D–v_{GS} characteristic of an NMOS transistor operating in the saturation region. The i_D–v_{OV} characteristic can be obtained by simply re-labelling the horizontal axis; that is, shifting the origin to the point $v_{GS} = V_{tn}$.

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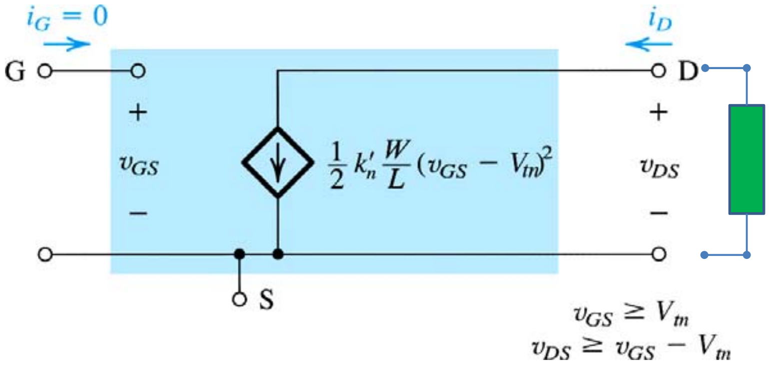
Large Signal Equivalent Circuit



Operating in Saturation

Ideal, back to this point later

Figure 5.15 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation

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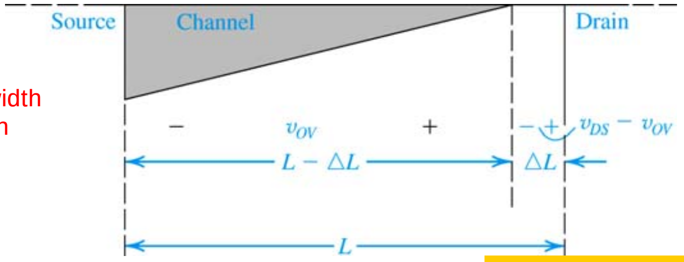
Finite Output Resistance



Channel width modulation

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{\enclose{circle}{L}}\right)V_{ov}^2$$

- As v_{DS} increases, the channel *pinch off* moves away from the drain (L gets smaller).
- Voltage across the channel remains v_{ov}
- A voltage drop of $v_{DS} - v_{ov}$ appears across the small depletion region
- This voltage accelerates the electrons that reach the drain (increases current)

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{ov}^2(1+\lambda v_{DS})$$

$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\text{ constant}}$$

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(V_{GS}-V_t)^2\right]^{-1}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{ov}^2(1+\lambda v_{DS})$$

i_D = 0 when v_{DS} =-1/λ= -V_A

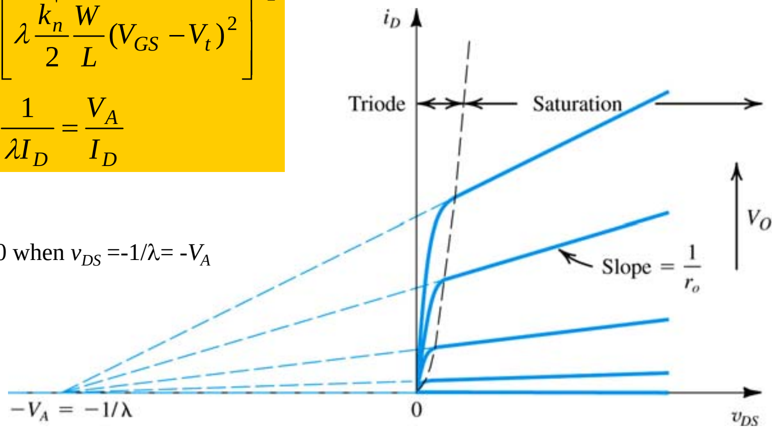


Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

Example

- Find R_s and R_d such that
- I_d=0.4 mA, V_D=+0.5 V
- V_t=0.7 V, $\mu_n C_{ox}$=100µA/V^2
- L=1µm, W=32µm.

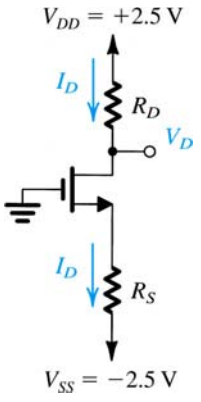


Figure 5.21 Circuit for Example 5.3.

Large Signal Equivalent Circuit

More realistic equivalent circuit

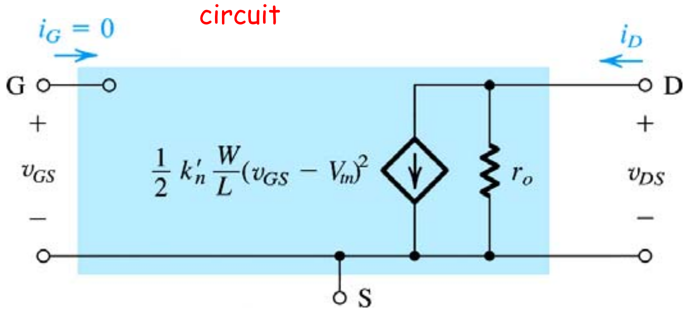
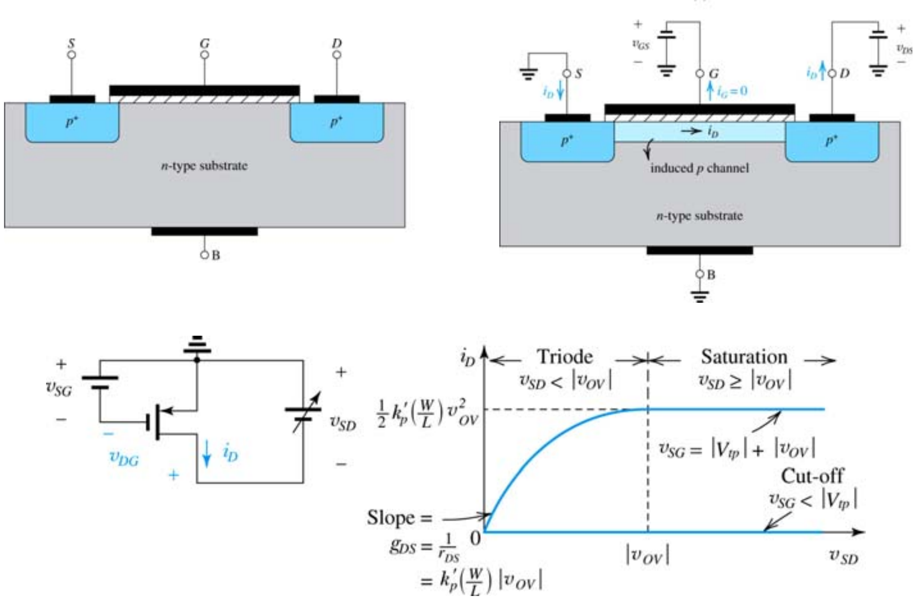


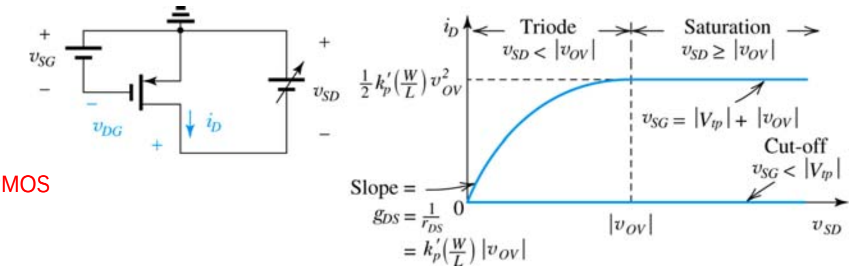
Figure 5.18 Large-signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (5.23).

PMOS

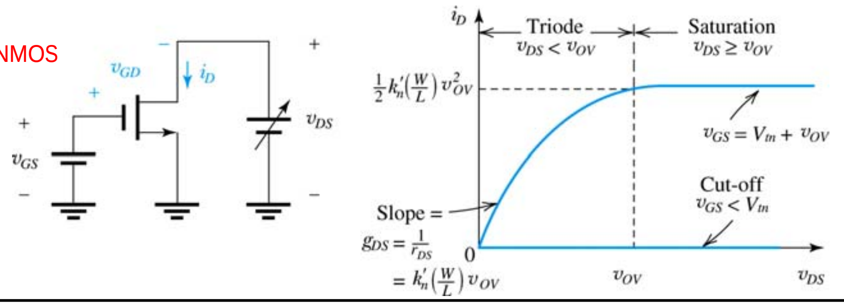


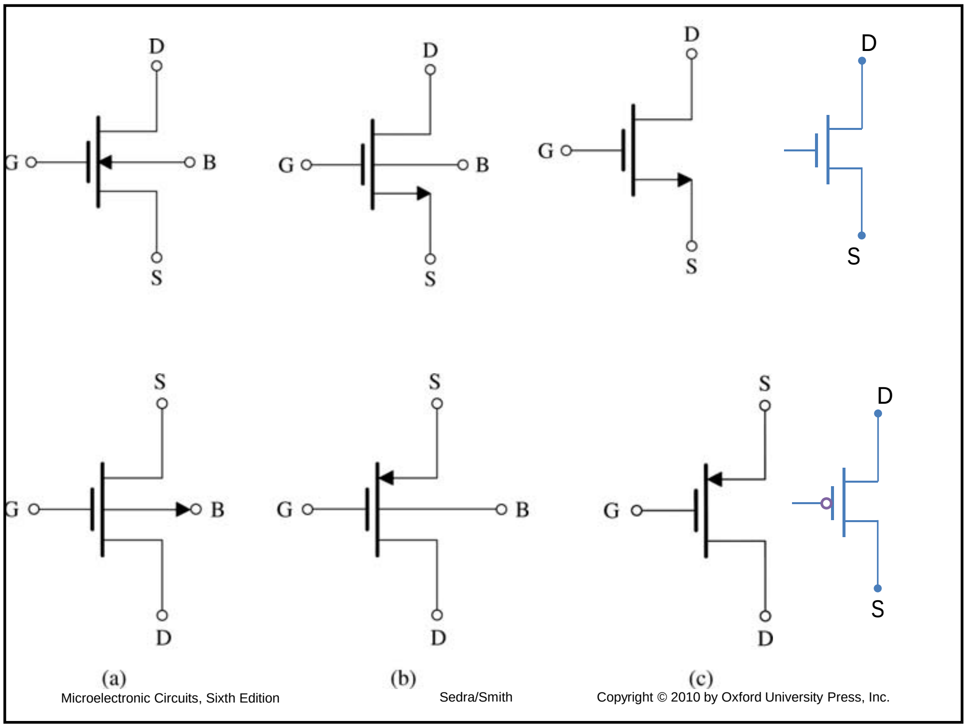
PMOS vs. NMOS

PMOS



NMOS





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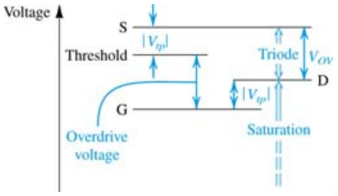
PMOS



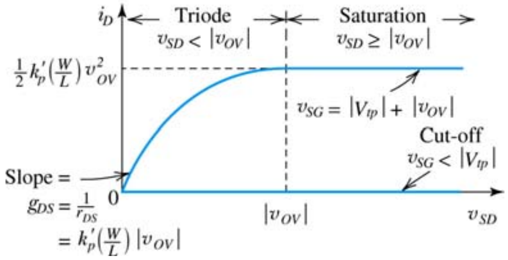
Cut-off

$$v_{SG} < |V_{tp}|$$

Saturation

$$v_{DG} \le |V_{tp}|$$

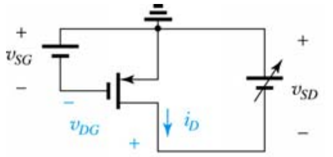
$$v_{SD} \ge |v_{OV}|$$



Triode

$$v_{SD} < |v_{OV}|$$

$$v_{DG} > |V_t|$$



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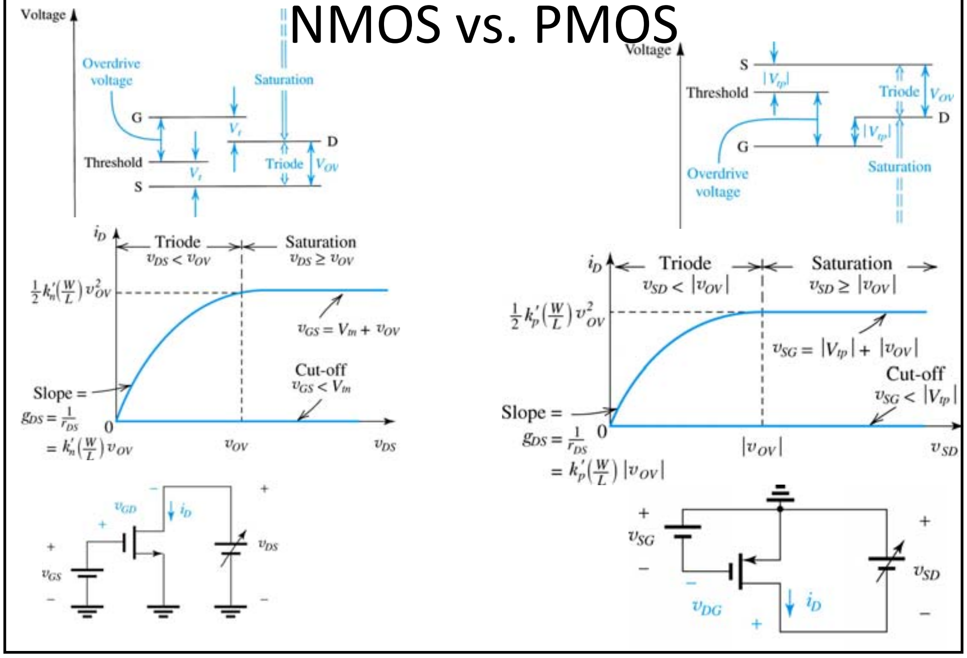
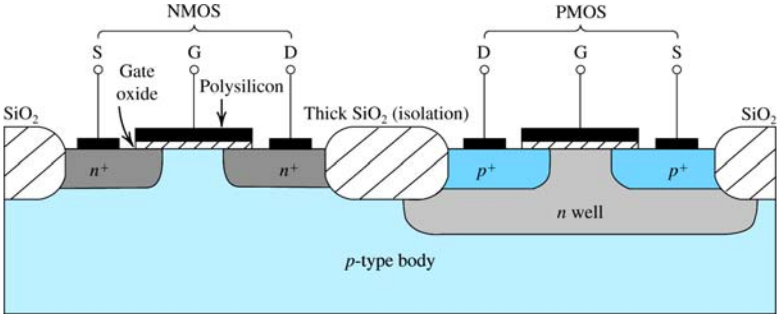
NMOS vs. PMOS



CMOS



The vast majority of IC's
Small and low power consumption

EXAMPLE

$V_{tp} = -1$ V, $K_p'=60\ \mu A/v^2$, W/L=10

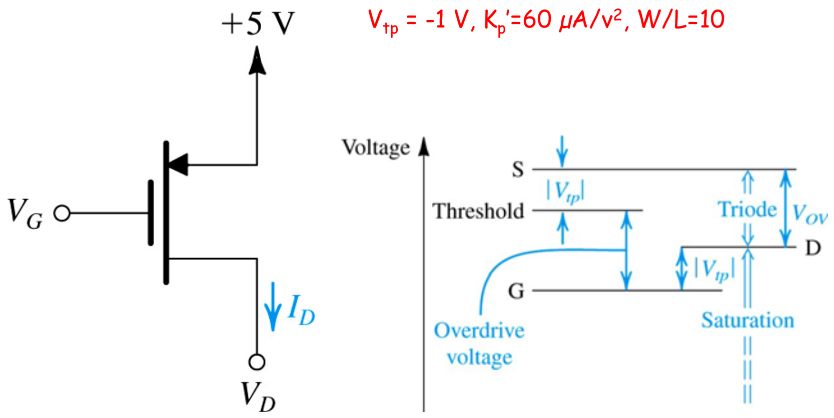
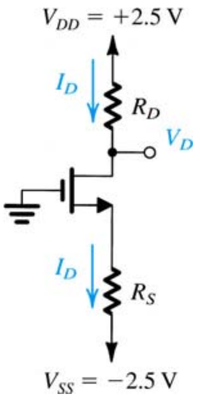


Figure E5.7



Find R_S and R_D such that $I_D = 0.4$ mA and $V_D = +0.5$V
Given
$V_t = 0.7$V, $\mu_n C_{ox} = 100\ \mu A/V^2$ and W/L = 32