York University
EECS 3201
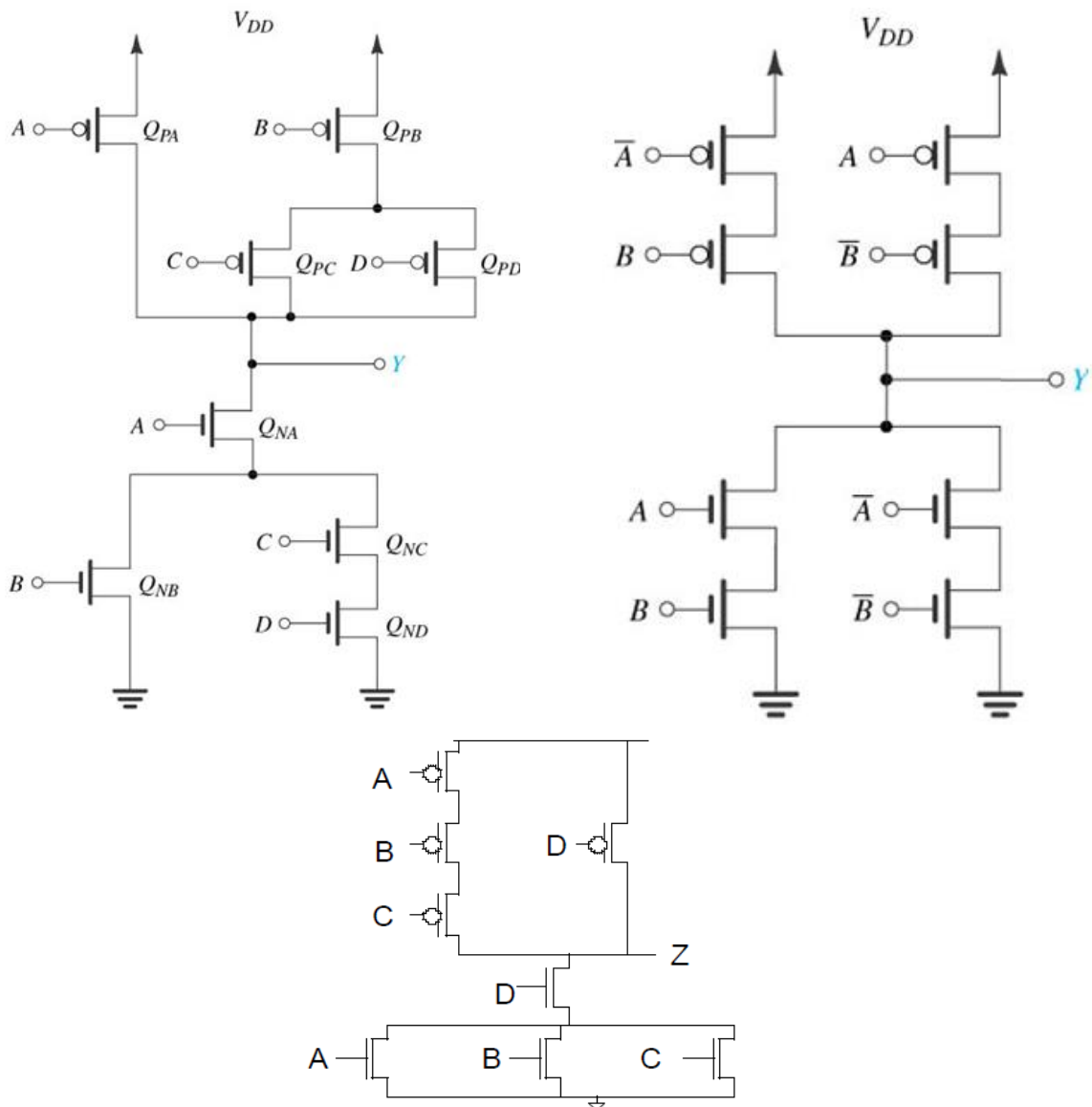Dr. Ihab Amer

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Assignment 1
(Due: October 20, 2014 – Please hand it to your TA during the lab session)

Exercise 1:

Derive the simplest Boolean expression for the circuits that are shown below. Start by constructing a truth table indicating which transistors are ON and which are OFF for all possible input combinations.

Exercise 2:

Find the number of dies per 20 cm wafer for a die that is 1.5 cm on a side if the number of dies in the area near the periphery of round wafers can be approximated by dividing the circumference of the wafer by the diagonal of the die. (This compensates for the "square peg in a round hole" problem.) Assuming that 50 of those dies were identified as "defected" during the testing processes, calculate the fabrication yield.

Exercise 3:

Solve the following from the end-of-chapter-1 problems of the textbook (Mano and Ciletti):

1.3.   (c) and (d)
1.5.   (c)
1.18. (c) and (d)
1.20. Note: Assume 7-bit operation, and indicate when/if an overflow occurs

Exercise 4:

Solve the following from the end-of-chapter-2 problems of the textbook (Mano and Ciletti):

2.2.   (f)
2.3.   (f)
2.9.   (b)
2.11. (b) Note: Solve this problem twice. First time, substitute directly to the simple logical expression, while in the second time, convert the expression to the canonical SOP format, and hence obtain the truth table
2.14. (a) and (e)
2.18.
2.29.
2.31.

Exercise 5:

Solve the following from the end-of-chapter-3 problems of the textbook (Mano and Ciletti):

3.2.   (d)
3.3.   (d)
3.4.   (f)
3.6.   (c)
3.12. (b)
3.15. (d)
3.16. (d)
3.18.