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EECS 3201: Guidelines for Final Exam

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Guidelines for the Final

Please read carefully before proceeding.

1. The duration of this exam is 180 minutes.

2. Point value of this exam is tentatively (45%).

3. Only un-programmable calculators are permitted for this exam.

4. You can use the back and/or the front of any exam sheet(s) (except pages 1– 4) for your scratch.

5. The exam consists of FORTY multiple choice questions, split among TWO parts, in FORTY THREE pages (including the cover). Please inform your proctor if you have any missing page(s) or question(s). You will lose the grade of any question(s) that are located in missing page(s).

Exam Strategy

Please insert all your answers for the exam in the table(s) that are provided in the next two pages (each part in its own page). Your grade in this exam will depend only on the answers that are indicated in the table(s). Tick (or cross) the table cell that corresponds to the answer that you believe is the most suitable.

More Guidelines

a. **If you solve any 36 out of the 40 questions correctly, you will get 100% of the total grade.**

b. Read all the *questions* **carefully**. For problems where Verilog HDL code is provided, pay attention to the comments inside the code and the modules' names.

c. Read all the *choices* **carefully**. There are choices that "*look*" alike, however they are obviously not!

d. This exam is designed so that the questions cover a broad range of difficulty-levels. **Manage your time** so that you do not lose the grades of the relatively-easy questions because of getting stuck at relatively-difficult questions.

e. Unless otherwise specified, assume that XILINX ISE XST (with default settings) is used for synthesis-related questions, while the simulator of Xilinx ISE is used for simulation.

f. Unless otherwise can be read from the waveforms, assume that shaded/patterned parts correspond to don't cares (X: unknowns).

g. Assume the existence of the following statement before all the given Verilog HDL modules: `` `timescale 1ns / 1ps ``

Exam Style!

- Broad selection of multiple choice questions based on topics delivered in all lectures
- Comprehensive exam (with focus on post-midterm material)
  - Pre-midterm material will mostly show-up in the form of Verilog HDL development/simulation
- Various types of problems
  - Theory
  - Problems to assess understanding of theoretical principles provided
  - Lots of Verilog! Maybe in the question(s) or the answer(s)!
  - Lots of Timing Simulations (and Synthesis)! Maybe in the question(s) or the answer(s)!
- Review your midterm exam

Final Advice!

- Do NOT freak out from the thick exam booklet. Many problems occupy more than one page due to space required for simulations, etc.
- Read question(s) well
- Read *all* choices. Pay attention to “None of the previous”, “All of the previous”, (i) and (ii), etc.
- Think first, don’t bang your head against the wall
- Good Luck!