1 SIMULATING WITH QSIM

1. The design **needs to be fully compiled**!

1.1 LIMITATION

Max simulation time is limited to **100 us only**!

1.2 GENERATING THE WAVEFORM

Start QSIM

In the displayed window select File -> Open Project

Browse to your Quartus project

Qsim command :

File -> New Simulation Input File.

This opens the 'waveform editor'

Default simulation time is of 800 ns; so, select Edit -> Set End Time, in the Waveform Editor

In the Waveform Editor window, select Edit -> Insert -> Insert Node or Bus.

In the pop-up window that appears, click on Node Finder.

In the open window, 'Pins: all' filter to select top level pins in your design. Use wildcard entry * as reqd.

To make it easier to draw the input waveforms, the Waveform Editor displays dashed grid lines. The spacing of the grid lines can be adjusted by selecting Edit -> Grid Size,

1.2.1 DRIVING A SIGNAL

Input waveforms can be drawn in different ways.

The most straightforward way is to indicate a specific time range and specify the value of a signal. To illustrate this approach, click the mouse on the x1 waveform near the 400-ns point and then drag the mouse to the 800-ns point.

Change the value of the waveform to 1 by clicking on the Forcing High (1) icon 

1.2.2 CLOCK SIGNAL

We will use a third approach to draw the waveform for x3. This signal should alternate between logic values 0 and 1 at each 100-ns interval. Such a regular pattern is indicative of a clock signal that is used in many logic circuits.

Even though there is no clock signal in our example circuit, it is convenient to specify x3 in this manner.

Click on the x3 input, which selects the entire 800-ns interval. Then, click on the Overwrite Clock icon 

1.2.3 SAVING WAVEFORM

Save the waveform file using a suitable name; we chose the name xyz_waveform.vwf. Note that the suffix vwf stands for vector waveform file.

File-> Save As (path defaults the project directory, which was open earlier)

1.3 RUNNING THE SIMULATION

Return to the Qsim window (in Figure 3). By closing the Simulation Waveform Editor.

Begin by clicking on Assign -> Simulation Settings... and specify the path to the vwf file you just created. Then, select Function (or Timing) as the Simulation Type.

To enable the functional simulation to be performed, it is necessary to generate a functional netlist of the circuit.

This netlist specifies the logic elements and the connections needed to implement the circuit. Select Processing -> Generate Simulation Netlist,

Now, we can simulate the circuit. Select Processing -> Start Simulation, or click on the icon