

Problem 1 (8 points)

Answer each of the following questions:

- (a) What is the minimum two's complement number that can be represented in six bits?

$$100000 = -32$$

- (b) What is the maximum two's complement number that can be represented in six bits?

$$011111 = 31$$

- (c) What does 11110001 represent in unsigned format?

$$2^0 + 2^4 + 2^5 + 2^6 + 2^7 = 241$$

- (d) What does 11110001 represent in 2's complement format

$$2^0 + 2^4 + 2^5 + 2^6 - 2^7 = \cancel{127} - 128 = -1$$

(e) Represent the number -2 in 4 bits using 2's complement format

$$\begin{array}{r} 0010 \\ + 1101 \\ \hline 1110 \end{array}$$

(f) represent the number 1 in 4 bits using two's complement format

$$0001$$

(g) Add the numbers in (e) and (f) using 2's complement, show the actual addition and what is the result?

$$\begin{array}{r} 1110 \\ + 0001 \\ \hline 1111 \end{array} \quad \boxed{-1}$$

Problem 2 (6 points)

Instruction	Cycles	percentage
load	4	20%
store	3	20%
add/sub	1	30%
multiply	10	10%
branch	3	20%

a) What is the average CPI?

7 pt.

$$4(0.2) + 3(0.2) + 1(0.3) + 10(0.1) + 3(0.2)$$

$$\boxed{3.3}$$

b) A program executes 10 billion instructions, and a clock rate of 500MHz, how long to execute this program on the above machine?

2 pt.

$$\frac{10 \times 10^9 \times 3.3}{500 \times 10^6} = 66 \text{ sec}$$

OR $10^{10} (4 \times 0.2 + 3 \times 0.2 + \dots) / 500 \times 10^6 = 66 \text{ sec}$

c) In order to improve the design, you have two choices; the first is to reduce multiplication time to 8 cycles. The second is to reduce store time to 1 cycle, but that means you have to increase branch by 1 cycle. Which one is faster? What is the increase in the performance for the fastest solution compared to the original CPU?

3 pt.

Case I

$$4(0.2) + 3(0.2) + 1(0.3)$$
~~$$+ 10(0.1) + 3(0.2)$$~~

$$3.1$$

Case II

~~$$4(0.2) + 3(0.2) + 1(0.3)$$~~
~~$$+ 10(0.1) + 3(0.2)$$~~

$$4(0.2) + 1(0.2) + 1(0.3)$$

$$+ 10(0.1) + 4(0.2)$$

$$2.8$$

Case II faster by

$$\frac{3.3}{2.8} = 1.18 \quad 18\%$$

$$\boxed{3.1}$$

Problem 3 (4 points)

A given application is written in Java runs 10 seconds on a desktop processor. A new Java compiler is released that requires only 0.5 as many instructions as the old compiler. Unfortunately, it increases the CPI by 20%. What is the percentage performance increase of this application using this new compiler?

$$T_{\text{before}} = 10 = IC \times CPI \times T_c \quad 2 \text{ pts}$$

$$\begin{aligned} T_{\text{after}} &= 0.5 IC \times 1.2 CPI \times T_c \\ &= 0.6 (IC \times CPI \times T_c) \\ &= 0.6 \times 10 = 6 \quad 2 \text{ pts} \end{aligned}$$

improves by $\frac{10}{6} = 1.66$ or 66%

Problem 4 (5 points)

Consider the following piece of code.

```

addi $s0, $zero, 6
addi $v0, $zero, -3
add $s1, $s0, $v0
beq $s1, $v0, skip
sll $s2, $s1, 1
skip
or $v0, $v0, $s2

```

$s0 = 6$
 $v0 = -3$
 $s1 = 3$
 not taken
 $s2 = 6$

Register \$s0 = 6
 Register \$v0 = -1
 Register \$s1 = 3
 Register \$s2 = 6

1 pt. each + 1

$v0 = v0 \text{ OR } s2$

$v0 = -3 = 2's \text{ complement } 000 \dots 011$

$11 \dots 1111101$

0000110

11111111

OR 6 = s2

= -1

Problem 5 (8 points)

Given the following code

Memory Address	Data Value
0x23180000	0x00000000
0x23180004	0x00000010
0x23180008	0x00001000
0x2318000C	0x00010000
0x23180010	0x00100000

Write the contents of the registers mentioned after the '#' after the execution of the instruction to the left

main:

```

lui $a0, 0x2318
ori $a0, $a0, 0x0000
lw $t0, 8($a0)
addi $sp, $sp, -4
sw $t0, 0($sp)
lw $t1, 0($a0)
or $t3, $t0, $t1
sw $t3, 0($a0)
addi $sp, $sp, -4
sw $t1, 0($sp)
lw $t3, 0($sp)
addi $sp, $sp, 4
lw $t4, 0($sp)
    
```

#\$a0 = 0x23180000
 #\$a0 = 0x23180000
 #t0 = 0x00001000
 #\$t0 = 0x00001000
 #\$t1 = 0x00000000
 #\$t3 = 0x00001000
 #\$t3 =
 #\$t3 = 0x00000000
 #\$t4 = 0x00001000

00001000
 00000000

Fill in the contents of the memory after the completion of the above code

Memory Address	Data Value
0x23180000	0x00001000
0x23180004	0x
0x23180008	0x
0x2318000C	0x
0x23180010	0x

} no change 1 pt.
 } no change 1 pt.

Problem 6 (4 points)

- ◆ In MIPS, there are many branch instructions `beq`, `bne`, `br`, `jr`. Which of these branches has the largest reach (can jump further away than any other branch)? Briefly explain.

`Jr` uses 32-bit register

- ◆ Name 2 different special purpose registers in MIPS and mention their use.

`SP` stack pointer

`FP` frame pointer

`at` compiler

`ra` return address

any 2 will do