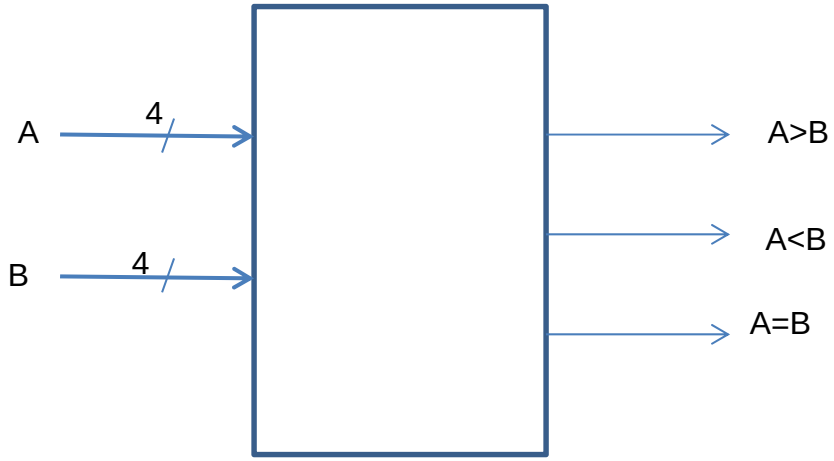
Sample lab test

The following 2 questions are sample problems to what you can find in the lab test.

The lab material is also a valuable source of examples to what could be in the lab test

By design, I mean write a Verilog module named Comparator. Please note that the automatic tester will assume the name of the file as indicated above with a .v extension

Design a 4-bit comparator. The inputs to the comparator are two numbers 4-bit each. The output are 3 outputs (<, >, =) one of these wires will be high (according to the values of the 2 numbers) and the other two are low (zero).



Modify the previous design such that

the inputs are 2 4-bit numbers, and a choice signal (2 bits) and only one output

If the choice is “00” the output is high if A==B, otherwise low (zero)

If the choice is “01” the output is high if A>B, otherwise low

If the choice is “10” the output is high if A<B, otherwise low

If the input is “11” the output is always 0