# Computer Science and Engineering 

## 2021 Sample Midterm

## Answer all questions in the space provided

Student Last Name: $\qquad$
Student Given Name: $\qquad$

Student ID. No: $\qquad$

| Section | Points | Marks |
| :---: | :---: | :---: |
| $A$ | 40 |  |
| $B$ | 40 |  |
| $C$ | 20 |  |
| Total | 100 |  |

## Section A

A1.
Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0 E 9 and has an execution time of 1.1 s , while compiler B results in a dynamic instruction count of 1.2 E 9 and an execution time of 1.5 s .
a) Find the average CPI for each program given that the processor has a clock cycle time of 1 ns .
b) Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?
c) A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?
a. CPU time $=$ Instruction count $\times$ CPI $\times$ Clock cycle time CPI = CPU time / (Instruction count $\times$ Clock cycle time)

Compiler A CPI $=1.1 /(1.0 \mathrm{E} 9 \times 1.0 \mathrm{E}-9)=1.1$
Compiler B CPI $=1.5 /(1.2 \mathrm{E} 9 \times 1.0 \mathrm{E}-9)=1.25$
b. $1 /$ Clock cycle time $=$ Instruction count $\times$ CPI / CPU time

Clock rate (Frequency) $=$ Instruction count $\times$ CPI / CPU time
For same CPU or execution time on both processors,
$\mathrm{f}_{\mathrm{B}} / \mathrm{f}_{\mathrm{A}}=($ Instruction count( B$\left.) \times \mathrm{CPI}(\mathrm{B})\right) /($ Instruction count $(\mathrm{A}) \times \operatorname{CPI}(\mathrm{A}))=1.37$
c. For the original processor with a clock cycle time of 1 ns :

$$
\begin{aligned}
(\mathrm{CPU} \text { time })_{\mathrm{A}} /(\mathrm{CPU} \text { time })_{\mathrm{NEW}} & =(\text { Instruction count } \times \mathrm{CPI})_{\mathrm{A}} /(\text { Instruction count } \times \mathrm{CPI})_{\mathrm{NEW}} \\
& =(1.0 \mathrm{E} 9 \times 1.1)_{\mathrm{A}} /(6.0 \mathrm{E} 8 \times 1.1)_{\mathrm{NEW}} \\
& =1.67 \\
(\mathrm{CPU} \text { time })_{\mathrm{B}} /(\mathrm{CPU} \text { time })_{\mathrm{NEW}} & =(\text { Instruction count } \times \mathrm{CPI})_{\mathrm{B}} /(\text { Instruction count } \times \mathrm{CPI})_{\mathrm{NEW}} \\
& =(1.2 \mathrm{E} 9 \times 1.25)_{\mathrm{B}} /(6.0 \mathrm{E} 8 \times 1.1)_{\mathrm{NEW}} \\
& =2.27
\end{aligned}
$$

A2.
Assume that registers $\$$ s0 and $\$$ s1 hold the values $0 \times 80000000$ and $0 x D 0000000$, respectively. What is the value of $\$$ to for the following assembly code?
add \$t0, \$s0, \$s1
add \$t0, \$t0, \$s0
$\$ t 0=0 x D 0000000$

A3.
Provide a minimal set of MIPS instructions that may be used to implement the following pseudoinstruction:
not \$t1, \$t2
nor \$t1, \$t2, \$t2
or
nor \$t1, \$0, \$t2
A4.
A5.

## Section B

## B1.

For the following C/Java statement, what is the corresponding MIPS assembly code? Assume that the variables $f$, $g$, and $h$ are given and could be considered 32-bit integers as declared in a C program. Use a minimal number of MIPS assembly instructions.

$$
f=g+(h-5)
$$

addi f, h, -5 (note, no subi)
add f, f, g

B2.
Give the binary representation of -67 in each of the following data representations
(a) 8-bit one's complement
(b) 8-bit two's complement
(c) hex

$$
01000011 \text { = +67 Decimal }
$$

a. $10111100=-678$-bit one's complement
b. $10111101=-678$-bit two's complement
c. $0 x b d=-67$ hex

## B3.

B4.

## Section C

## C1.

For the MIPS assembly instructions below, what is the corresponding C/Java statement? Assume that the variables $\mathfrak{f}, \mathrm{g}, \mathrm{h}, \mathrm{i}$, and j are assigned to registers $\$ \mathrm{~s} 0, \$ \mathrm{~s} 1, \$ \mathrm{~s} 2, \$ \mathrm{~s} 3$, and $\$ \mathrm{~s} 4$, respectively. Assume that the base address of the arrays $A$ and $B$ are in registers $\$ s 6$ and $\$ s 7$, respectively.
sil \$t0, \$s0, 2
add \$t0, \$s6, \$t0
sll \$t1, \$s1, 2
add \$t1, \$s7, \$t1
Iw \$s0, 0(\$t0)
addi \$t2, \$t0, 4
lw \$t0, 0(\$t2)
add \$t0, \$t0, \$s0
sw \$t0, $0(\$ 11)$

$$
\mathrm{B}[\mathrm{~g}]=\mathrm{A}[f]+\mathrm{A}[1+\mathrm{f}] ;
$$

C2.
Provide the type, assembly language instruction, and binary representation of instruction described by the following MIPS fields:


C3.
C4.

