Interconnection Networks

EECS4201 Fall 2016 York University

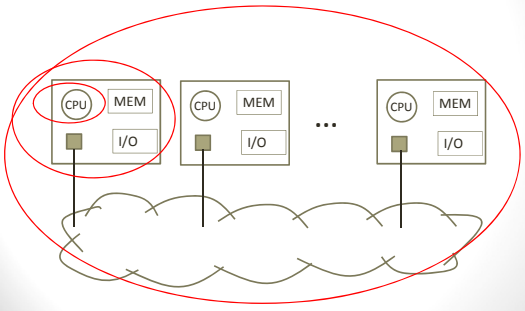
1

Introduction

- In multiprocessors connecting different processors together
- On chip connecting CPU to memory banks and I/O
- On chip connecting cores to caches in the CPU
- Effect on Scalability, power, performance, and eventually cost.
- Topology, routing and flow control (buffering)

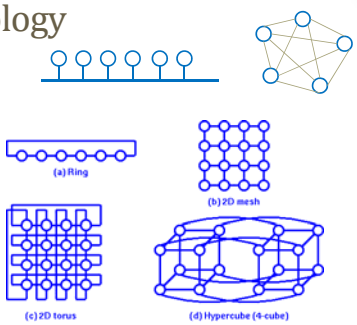
2

Interconnection Networks



3

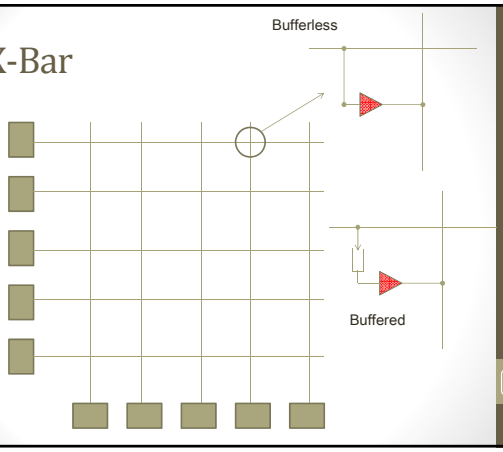
Topology



Source: cis.k.hosei.ac.jp (google images)

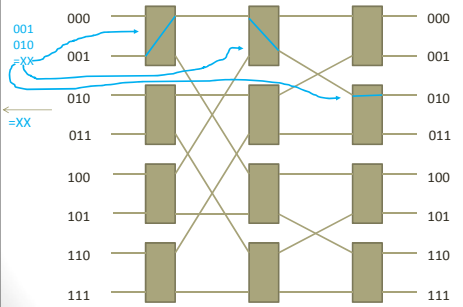
4

X-Bar



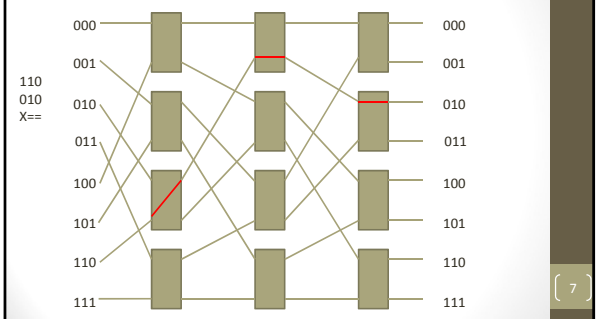
5

Multristage O(logn)Δ



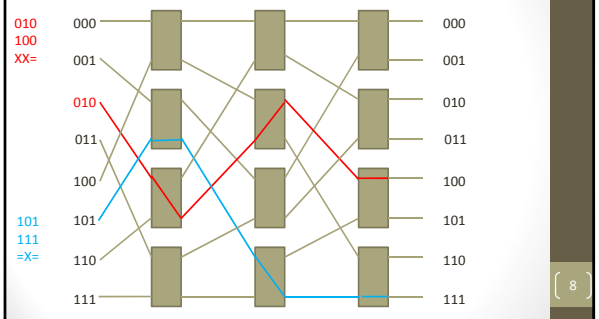
6

Omega Network

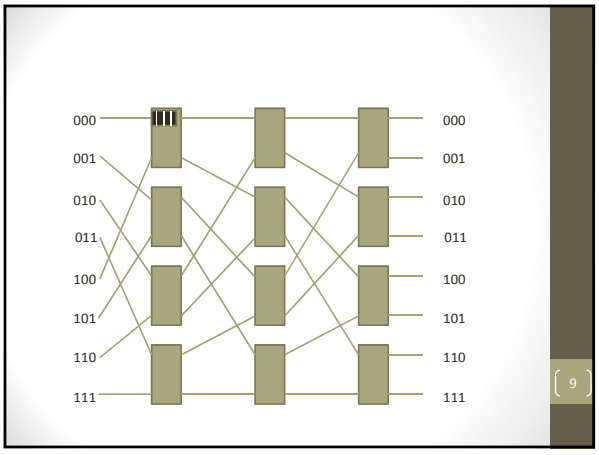


7

Omega Network

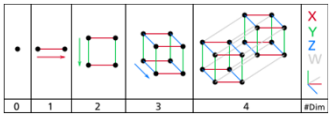


8



9

Hypercube Networks

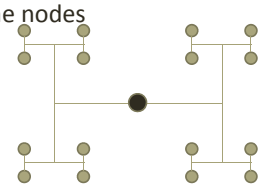


By NerdBoy1392 - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=5514315

10

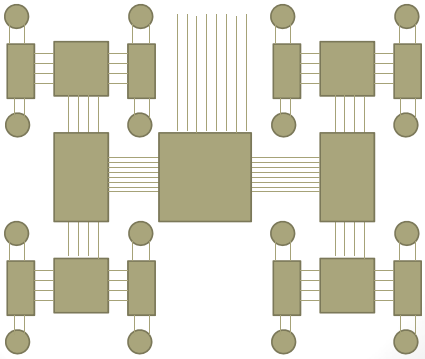
Trees

- O(logn)
- Communication is local --> very good
- Root is more congested than the rest of the nodes



11

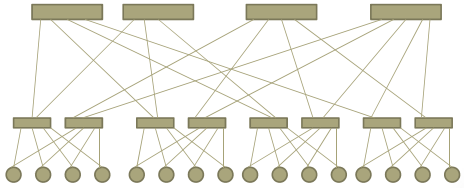
Fat Trees



12

Fat Trees

- Point-to-point, multicasting reduction, randomized routing



13

Hierarchical Networks

- Network of networks
- Connected cube cycles (CCC), MLH, …….
- More scalable
- More complex
- More than one level of routing
- Usefule if communication is localized

14

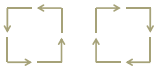
Routing

- Deterministic: Each path is set beforehand, no changes are made to the path
  - Simple
  - Can not avoid congestion
  - Dimension order routing
- Adaptive: Changes are made to the route based on faults and congestion
  - More complicated router
  - Can avoid congestion
- Deadlock and how to avoid it.
- Circuit vs. packet switching

15

Deadlock

Deadlock may occur if we allow these turns



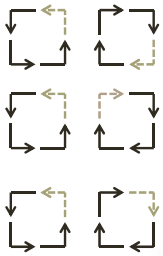
Dimension order routing

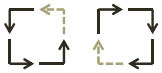
- A cycle of resource dependence.
- Every one is waiting for the release of a resource, the last one is waiting for the release of the first one.
- Resources are mainly buffers.

16

Avoiding Deadlock

- We have to break the cycle
- West first





17

Message/Packet/Flit

- Messages are exchanged between nodes
- Messages are divided into packets
- Packets may use different paths and are assembled at destination (need overhead for reassembly).
- 2 packets from the same message may take different paths from A $\rightarrow$ B
- A packet is divided into flits, all filts in a packet takes the same route (no header per flit)

18

Switch Architecture

19

Flow Control

- Packet switching vs circuit switching
- Need to buffer or not
- How to reserve buffers
- Cut-through vs. store-and –forward (first receive THHHHD then start forwarding)

20

Physical vs. Virtual Channel

- Physical Channel

- Virtual channel (same physical channel)

21