Paper/Topic survey

In this part of the course, you have to choose a paper and write a review/critique for this paper.

The paper review should be 1-3 pages. Size doesn't matter; it is what you include in the review that counts. The paper should be (loosely) organized as follows:

1. Summary: summarize the paper mentioning what is the main point the author wanted to address.
2. Strength: What do you like about this paper the most? Did the author solve the problem he/she wanted to? was the solution/improvement incrementally (just slight improvement from a previous work) or a major improvement?
3. Weakness: What would you have done if you are doing this research differently? Did the author ignore something you would have wanted him to address?

How to write/review a paper

1. Roy Levin and David D. Redell, How (and How Not) to Write a Good Systems Paper
2. Mark D. Hill Oral Presentation Advice I know you will not present the review, but wouldn't hurt to know this
3. Mark Hill and Kathryn S McKinley Notes on Constructive and Positive Reviewing

Choosing the paper

You can choose the paper based on topics, some major conferences/journals, or from the list supplied here. The list is by no mean inclusive, it is just few examples from the conferences and journals mentioned below.

Major Journals and Conferences

The major conferences in computer architecture are ISCA (International Symposium on Computer Architecture) MICRO (The Annual IEEE/ACM International Symposium on Microarchitecture). IEEE Micro (journal), IEEE Computer, IEEE Transactions on Computer Architecture. You can use IEEExplore.ieee.org (free from a computer in our university domain) to get to any of the above journals/conferences

By Topic

The topic of the paper should be related (even remotely) to computer architecture. Few examples are Computer architecture, DRAM, embedded systems, security (the hardware or embedded side), cache organization, special purpose hardware, ….

List of papers

Here are some papers that you can consider for the paper review. If you have any other ideas, please discuss it with me.

1. T-Y. Yeh and Y. Patt. Two-level Adaptive Training Branch Prediction, *ISCA 1991*. Reprinted in HJ&S pp. 228-237
2. S. Parameswaran , and T. Wolf, "Embedded systems security—an overview" . Des Autom Embed Syst (2008) 12: 173–183.
3. Kornecki, A.J.; Zalewski, J.; Stevenson, W.F. "Availability Assessment of Embedded Systems with Security Vulnerabilities" Software Engineering Workshop (SEW), 2011 34th IEEE
4. Zafar, S.; Dromey, R.G. Integrating safety and security requirements into design of an embedded system. Software Engineering Conference, 2005. APSEC '05. 12th Asia-Pacific
5. Koka, P. ; McCracken, M.O. ; Schwetman, H. ; Chen, C.-H.O. ;Xuezhe Zheng ; Ho, R. ; Raj, K. ; Krishnamoorthy, A.V. "A micro-architectural analysis of switched photonic multi-chip interconnects" ISCA 2012, Page(s):153 - 164
6. Kshitij Sudan, Saisanthosh Balakrishnan, Sean Lie, Min Xu, Dhiraj Mallick, Gary Lauterbach, Rajeev Balasubramonian "A Novel System Architecture for Web Scale Applications Using Lightweight CPUs and Virtualized I/O" HPCA 2013
7. Efficiently Prefetching Complex Address Patterns, Manjunath Shevgoor, Sahil Koladiya, Rajeev Balasubramonian, Seth Pugsley, Chris Wilkerson, Zeshan Chishti, *48th International Symposium on Microarchitecture (MICRO-48)*, Hawaii, December 2015.
8. D. Joseph and D. Grunwald, "Prefetching Using Markov Predictors," in Proceedings of ISCA, 1997.
9. [ISCA] "Towards Energy Proportionality for Large-Scale Latency-Critical Workloads," David Lo, Liqun Cheng, Rama Govindaraju, Luiz Barroso, Christos Kozyrakis *Proceedings of the 41st Intl. Symposium on Computer Architecture (ISCA)*, Minneapolis, MN, June 2014. [PDF] [slides]
10. Shekhar Borkar, Designing Reliable Systems from Unreliable Components: The Challenges of Transistor Variability and Degradation, *IEEE Micro 2005, November/December 2005 (Vol. 25, No. 6) pp. 10-16.*
11. Bruce Jacob and Trevor Mudge. Virtual Memory on Contemporary Processors, IEEE Micro, vol. 18, no. 4, 1998.