# York University

# Dept. of Electrical Engineering and Computer Science

EECS4201
Computer Architecture
Name _____ Quiz 3 ID_____
Dec. 1, 2016
Time allowed: 15 minutes

## Question 1 – 8 points

Consider a Cray-like SIMD machine; we would like to perform the following addition on two vectors (of course we have to load them from memory first).

V1 <- V2 + V3

Assuming a memory latency of 10 cycles (you get the first element after 10 cycles), a pipelined adder latency of 6 cycles and vector length = 64.

a) Assuming chaining and 2 memory modules (also assume that the vectors are properly stored to minimize memory access time)

**Load V1 0 → 73**

**Load V2 1 → 74**

**Add starts at 12**

**12+5+63= 80 cycles**

b) Assuming chaining and one memory module, how long to complete the addition?

**Load V1 0 → 73**

**Load V2 74 → 74+10+63**

**Add starts at 74+10=84**

**84+5+63= 152 cycles**

## Question 2 – 2 points

Again, a cray-like machine. if we have this peace of code

```
for(i=0; i<64; i++)
     if(V[i] != 0)  V[i] = 2*v[i];
```

If you know that 10% of the vector components are 0, assume un-pipelined multiplier (only 1 cycle).

How many multiplication cycles are used to to finish the above code?

**masking will still perform the operation, no savingto the destination register though**

**The answer is 64**