EECS4201E

Assignment 4

Due Last day of classes

Consider the following loop

```
Loop:  LD    F0, 0(R1)
       FMUL  F4, F0, F6
       FADD  F4, F4, F2
       ST    F4, 0(R1)
       ADDI  R1, R1, -8
       BEQ   R1, R2, loop
```

Problem 1

Assume no prediction and single issue, schedule the first three iterations of this loop stating the time every instruction is issued, start execution finished execution and write back the result. Assume addition and integer operations takes one cycle, floating point multiplication takes three cycles.

Use the format we used in the slides, if the instruction takes more than one cycle in the execution stage, state the cycles, consider the following example.

Instruction	issued	execution	memory	CDB write
LD	1	2	3	4
FMUL	2	5,6,7		8

Problem 2

Repeat problem one with 2-issue processor.

Problem 3

Repeat considering VLIW processor that can issue a maximum of 2 memory operations, 2 floating point operations and one integer operation per instruction. Consider the following latencies

Load followed by FP or integer operation	1 cycle
FP add followed by another FP store	2 cycles

FP op followed by another FP op 3 cycles.

Use loop unrolling to achieve no-stall execution. How many times we have to unroll the loop?

Problem 4

Use vector processing to do the loop, assume all vectors have a length of 64. Memory latency is 10, FP adder latency of 4, MUL latency of 6.

By latency we mean when accessing the memory, the first element is available after 10 cycles. Assume also the memory has 2 read ports and one write port.