EECS 3216

Winter 2021

LAB 2

UP-DOWN SAWTOOTH COUNTER

Lab Objective

In this lab, you will implement a finite state machine to implement a counter.

LAB

Design an up-down sawtooth counter, the counter operation is as follows

0 → 1 → 2 → 3 → 4 → 5 → 6 → 7 → 6 → 5 → 4 → 3 → 2 → 1 → 0 → 1 and so on

Specifications

1. The counter output is 3 bits
2. The output is displayed on the right-most three LED's
3. The display frequency is 1 Hz (updates once every second).
4. The output is displayed on LEDR2 LEDR1 LEDR0 (right most three LED's, with the right-most LED is the lease significant bit).

Deliverables

1. A report containing the following
    a. Your name, student number, and Lab number
    b. Design: How did you reach your implementation. For this lab, you can use English, FSM, tables, or pseudo code. You must specify what will be the duty cycle for all the settings of the switches. You also must explain/show any fixed numbers in your design (A 5-bit counter, why did you choose 5?)
    c. Verilog code
    d. A testbench for your code
    e. Modelsim simulation results (the waveforms).
2. A video (10 seconds) in the video you show your circuit working

Marking

Video presentation (50%), the report (50%). For each the marks are 3, 2, and 1. For doing everything you were asked to, most of what you are asked to do, less than half, or non at all

The lab is due 11:59 pm February 10.