EECS 3216

Winter 2021

LAB 3

TRAFFIC LIGHT CONTROLLER

Lab Objective

Making a timed FSM to solve a specific problem

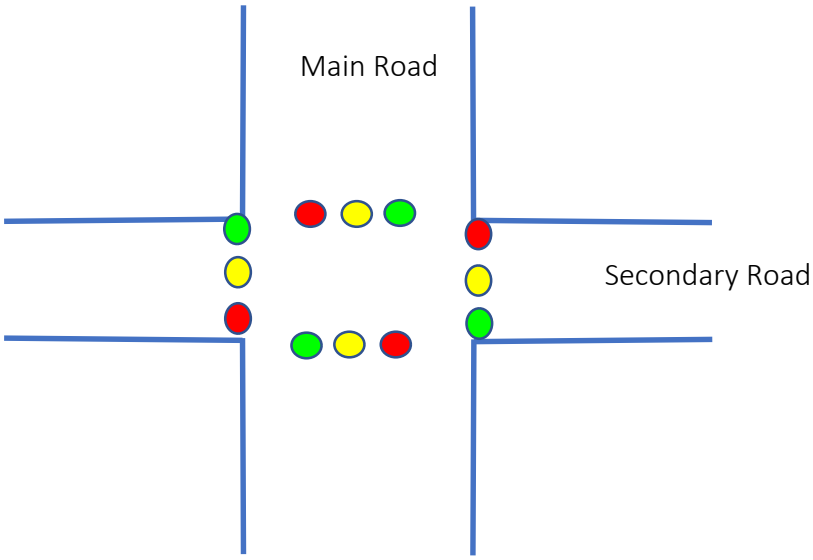
Implementing the FSM as a Verilog code and testing it on the DE-10 Lite board

LAB

Design a traffic light controller to control the traffic light shown below. There are 4 traffic lights, but every two of them work in synch (no left turn or right turn signals).

Normal operation is the main road light is green and the secondary road light is red. There is a cross request signal and a car sensing signal on the secondary road. When either of these signals are generated (by pushing a switch or from the car sensor) the main road signal becomes yellow (possibly after some time) then red, and the secondary road signal becomes green. There is no delay between the main/secondary going red and the secondary/main going green.

The exact specification is given below, keep in mind that might not be very practical specification because we shortened the time in order to make the presentation video short



Specifications

1. Normal operation is a cycle of Secondary Red, and Main Green for 10 sec, followed Main Yellow for 2 seconds, then Main Red for 7 second (during these 7 seconds, Secondary is Green for 5 seconds, then yellow for 2 seconds) then Secondary Red again and the whole cycle is repeated
2. There is a pedestrian cross request button and a car sense in the secondary road. If either is activated, that shortens the main road Green time.
3. When either the cross or car sensor is triggered, the time is shortened by 5 seconds. If the remaining time is less than 5 seconds, nothing changes.
4. Inputs: there are two input signals
    a. Reset signal rst to reset the lights to Main Rd Green and start counting SW0
    b. Car sensor Ored with pedestrian request SW1
5. Outputs:
    a. Main Red LEDR0
    b. Main Yellow LEDR1
    c. Main Green LEDR2
    d. Sec. Red LEDR3
    e. Sec. Yellow LEDR4
    f. Sec. Green LEDR5
    g. The number of seconds remaining in the cycle is displayed on one of the seven segment display

Deliverables

1. A report containing the following
    a. Your name, student number, and Lab number

   b. Design: How did you reach your implementation. For this lab use FSM. You must explain/show any fixed numbers in your design (A 5-bit counter, why did you choose 5?)
   c. Verilog code
2. A video that shows your circuit working

Marking

Video presentation (50%), the report (50%). For each the marks are 3, 2, and 1. For doing everything you were asked to, most of what you are asked to do, less than half, or non at all

The lab is due 11:59 pm February 21.