EECS 3216

Winter 2021

LAB 6

TESTING AND VERIFICATION

Lab Objective

To introduce students to testing and verification of digital systems.

Introduction

In this lab, you have to produce testbenches for testing and verification of lab 3.

We didn't cover verification yet (we will start this Tuesday), so stay tuned for details

Testing

In this lab, you have to design a testbench to test your lab 3 code. You have to use assertions.

First, you have to decide what are the properties you want to test. choosing the properties is a part of the lab, and you will be graded on it. Testing unnecessarily or not testing enough means mark deduction. You have to understand the problem, then

decide what you want to test. Then you have to write systemverilog code to test it. Since there is no simulator to run, you are not responsible for small syntax error (forgetting a semicolon is OK, fforgetting to end a module is NOT).

Deliverables

A report stating your testing plan, and the systemverilog code to implement it

The lab is due 11:59 pm April 8.